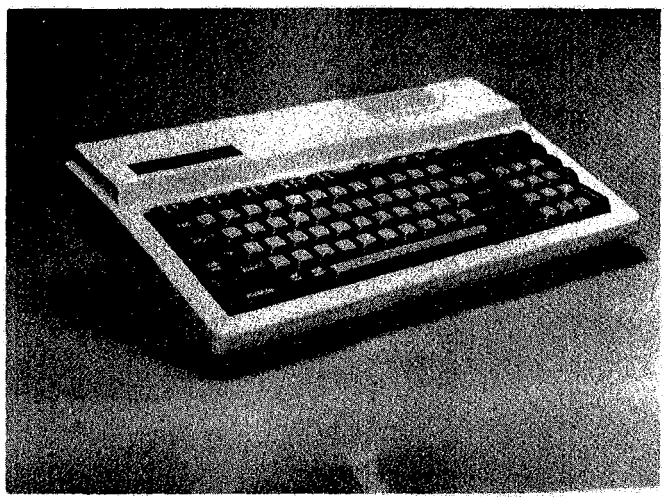
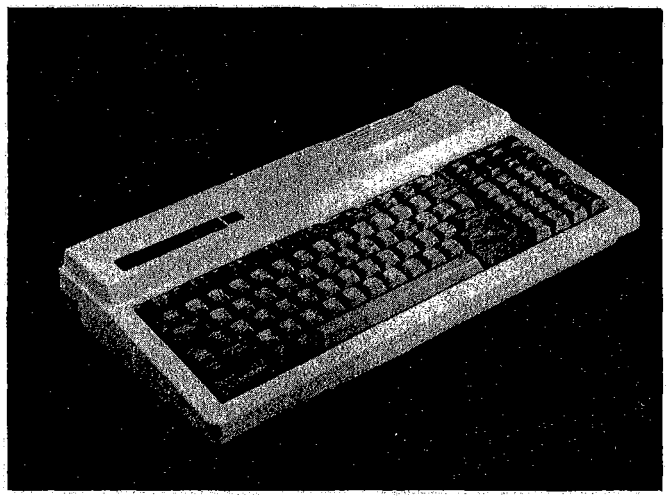
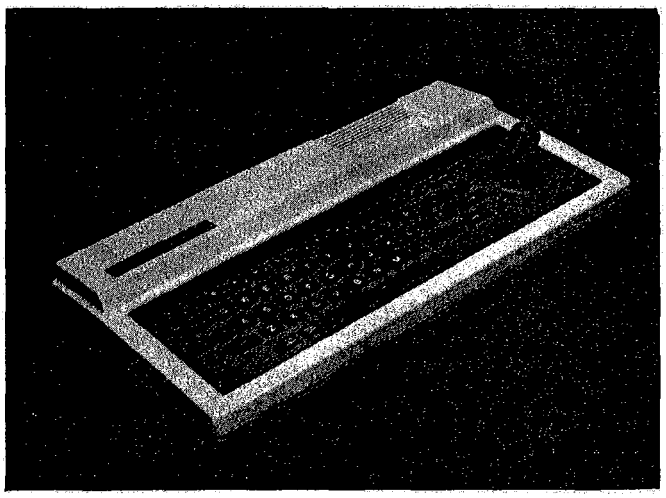
SERVICE & TECHNICAL MANUAL (VOL. 1)

SVI 318/328 (MKI/MKII) COMPUTER SYSTEM







SVI
SPECTRAVIDEO

Service/Technical Manuals (SVI-318/SVI-328) and Mark II

Section:

1. General Description
2. System Introduction
3. Diagnostic Test and Trouble Shooting Chart
4. Theory of Operation Description
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6. Spare Parts List and Recommended Spare Parts List
7. Appendix

Circuit Schematic:

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E. Schematic Diagrams of SVI-903 Data Cassette and SVI-904 Mono Data Cassette

F. Schematic Diagrams of SVI-603 Game Adaptor

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1. GENERAL DESCRIPTION

SCOPE

This manual is designed to assist a trained engineer in locating and correcting problems that may occur with the SVI-318/SVI-328 and Mark II. Specially developed self-study and training courses are available from Spectravideo International Ltd. (hereinafter referred as 'SVI'), and before attempting to service the computer the engineer should have completed one of these courses.

FEDERAL COMMUNICATIONS COMMISSION RADIO FREQUENCY INTERFERENCE STATEMENT

WARNING: This equipment has been certified to comply with the limits for a Class B computing device, pursuant to Subpart J of Part 15 of FCC rules. Only peripherals (computer input/output devices, terminals, printers, etc.) certified to comply with the Class B limits may be attached to this computer. Operation with non-certified peripherals is likely to result in interference to radio and TV reception.

(SVI) SPECTRAVIDEO INTERNATIONAL LTD., HONG KONG

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This document contains the latest information available at the time of publication. However SVI reserves the right to modify the contents of this material at any time. Also, all features, functions, and operations described herein may not be marketed by SVI in all parts of the world. Therefore, before using this document, consult your nearest dealer or SVI for the information that is applicable and current.

CHARACTERISTICS

The following lists the characteristics of and accessories for SVI-318/ SVI-328 home computer. Refer to this section during any procedure that requires checking the computer against its performance or power specifications.

POWER SOURCE	AC 115V +-10% 60 Hz AC 200V +-10% 50 Hz AC 220V +-10% 50 Hz AC 240V +-10% 50 Hz
POWER CONSUMPTION	17W (excluding optional interfaces and peripheral devices) 14W (Mark II)
TEMPERATURE	Operating 0° - 35°C (32°F - 95°F) Storage 15° - 60°C (5°F - 140°F)
HUMIDITY	Service humidity 80% or less
DIMENSIONS (mm)	405 (L) x 218 (W) x 77 (H)
WEIGHT	4 Kg

OPERATOR INTERFACE

The status indicator lights tell when power is applied to the computer, when the computer is busy doing calculations, when the computer is performing input/output operations, and when waiting to stop at the end of the current Micro-soft Basic language instruction in response to pressing the stop key.

User-definable function keys allow the operator to branch to any of ten specified BASIC programme locations when pressing one of these keys. There are ten keys to specify ten programme locations. Another ten locations are used if the keys are pressed in conjunction with holding down a SHIFT key.

The alphanumeric keyboard is used for entry of BASIC programme language statements and date. The numeric keypad provides convenience when entering numeric data into the computer. The basic calculator functions are also readily available. When used as a calculator without running a Basic programme, the ENTER key causes the calculated result to print on the display.

POWER SWITCH

The power switch is a rocker switch used for applying power to the SVI-318/SVI-328 and Mark II.

POWER INDICATOR

The power indicator is an LED that monitors the +5V supply. When on, it indicates the presence of power to the SVI-318/SVI-328 and Mark II.

2. SYSTEM INTRODUCTION

This manual is arranged in the following sections:

1. General information about the SVI-318/SVI-328 and Mark II personal computer and its peripherals, including model number and feature kit descriptions.

2. Information on how to remove and replace the major assemblies that make up the computer.

3. How to use the diagnostic module, an explanation of the diagnostic messages and which parts to replace.

4. Tables and charts showing plug/pin assignments, test points and the location of the major components on the controller board.

5. Schematices and parts identification information.

   For detailed information on how to repair the disk drives, printers, or any other peripherals refer to the approperiate service publication.

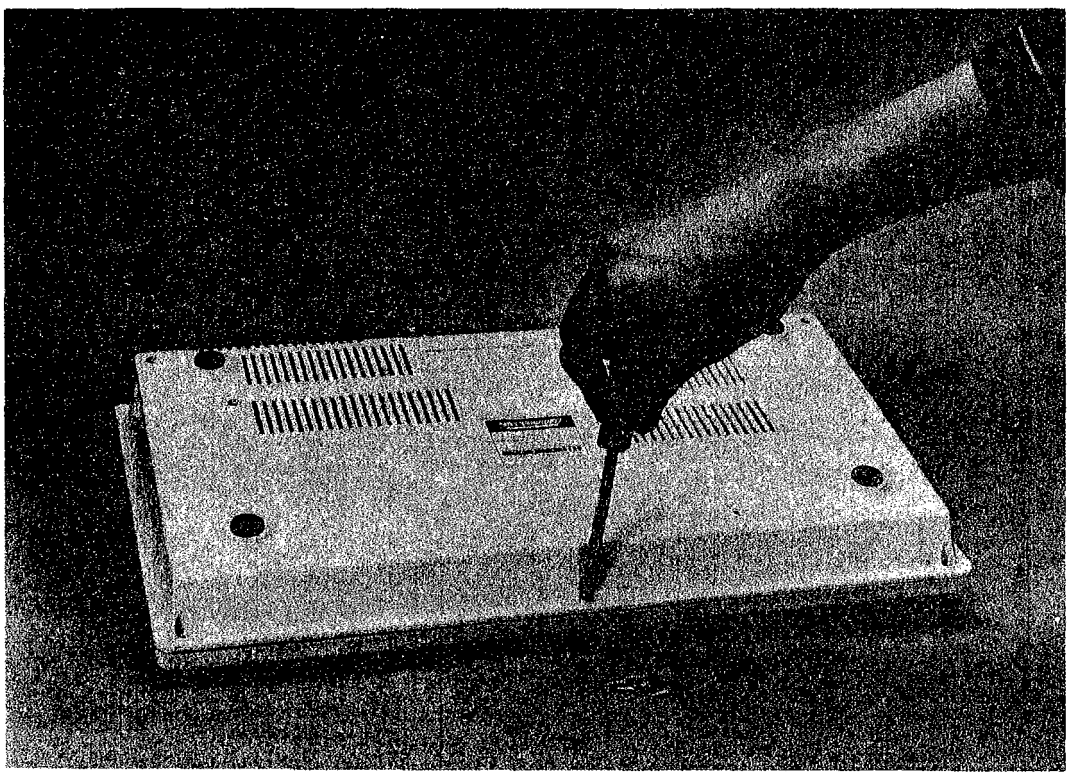
To remove the cover refer to Figure 2-1 and use the following procedures.

1. Be sure the on/off switch is in the off position.

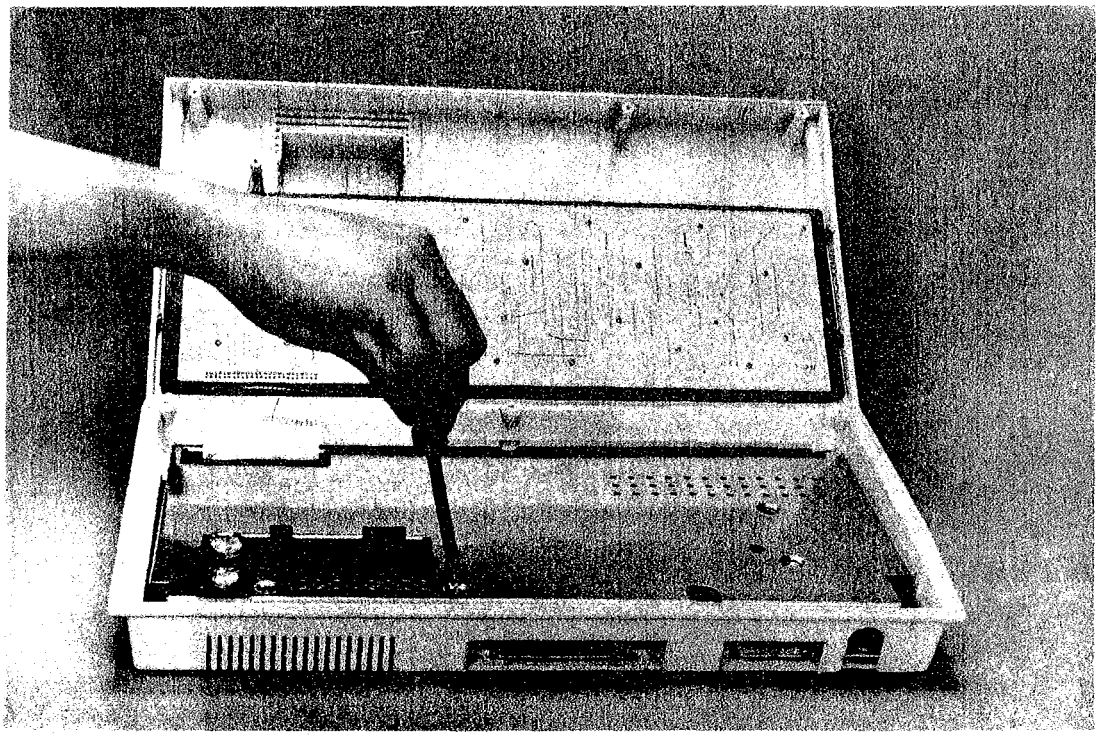
2. Disconnect the power supply.

3. Disconnect any peripherals.

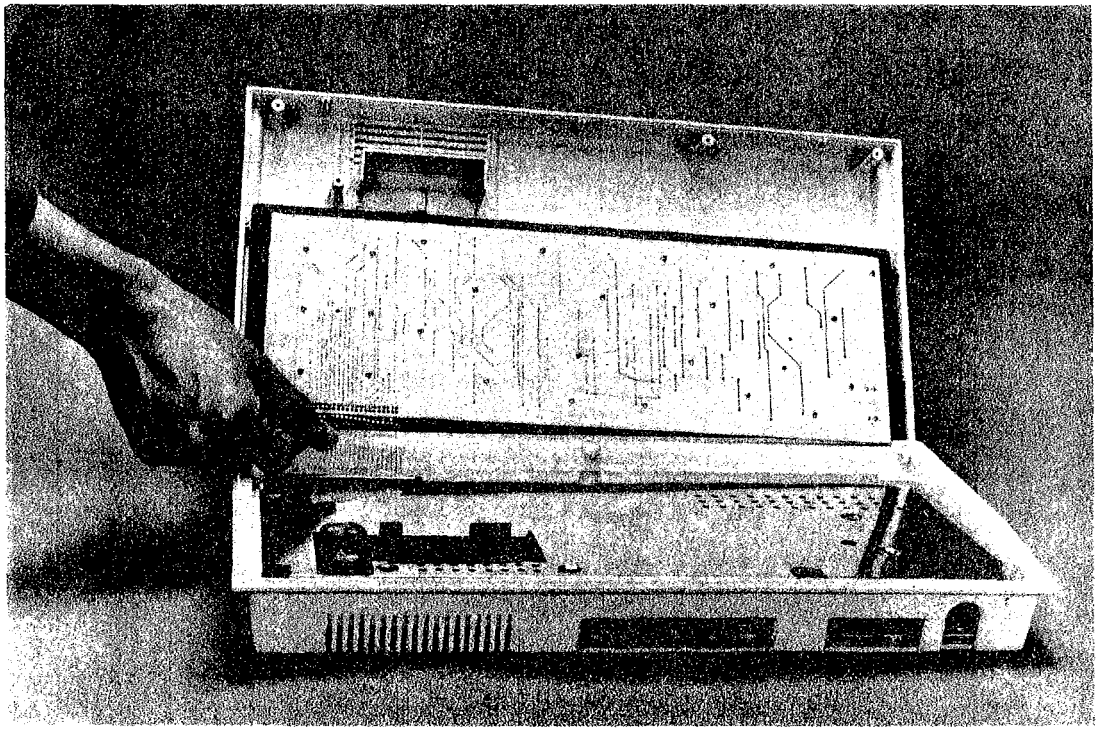
4. Remove the seven retaining screens.



4. Remove the seven retaining screens.

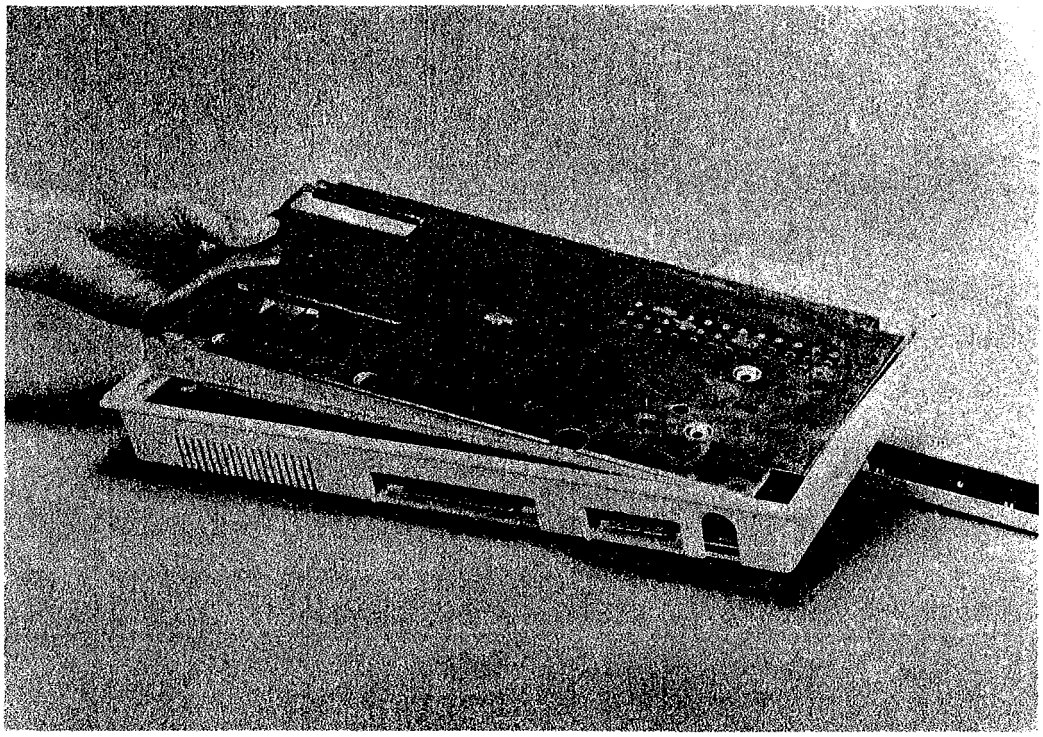


5. Remove the cover.

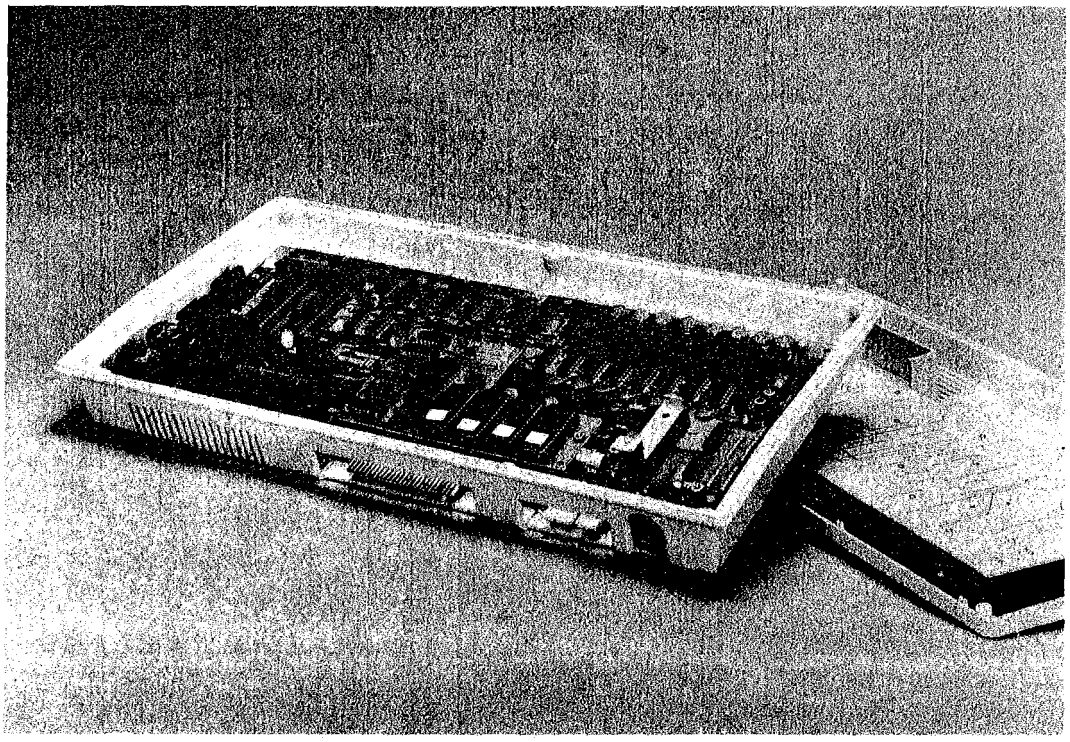


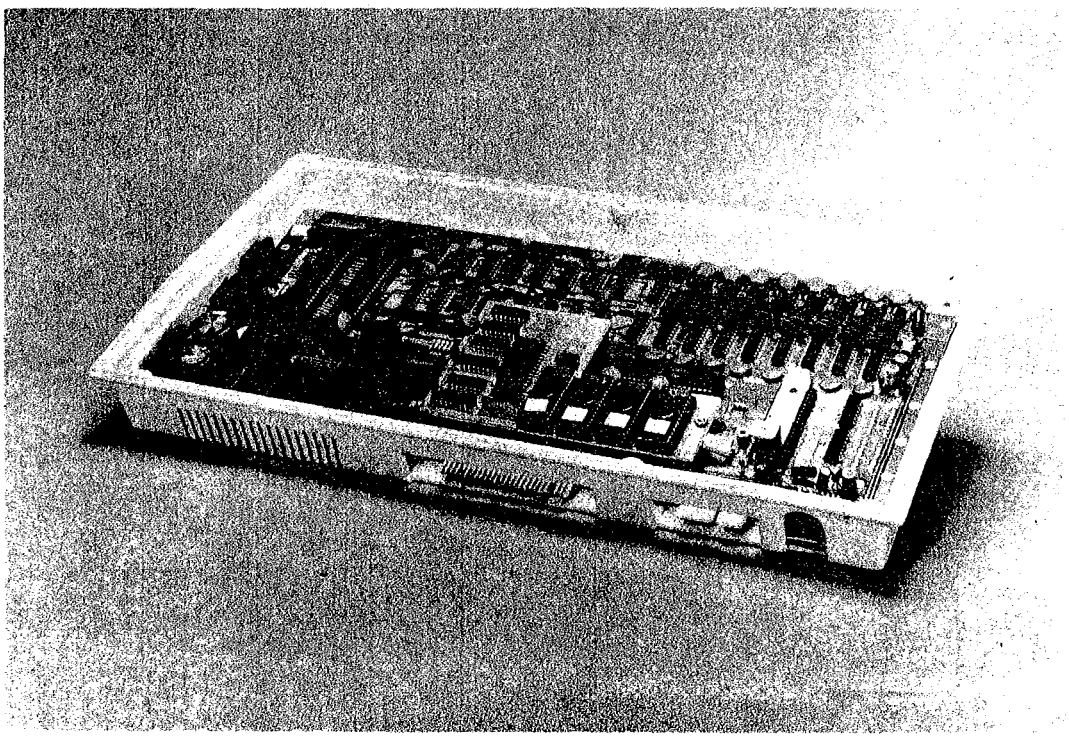
6. Remove the screens on the metal cover.

7. Remove the metal cover.



To re-assemble, use the above procedures in the reverse order.



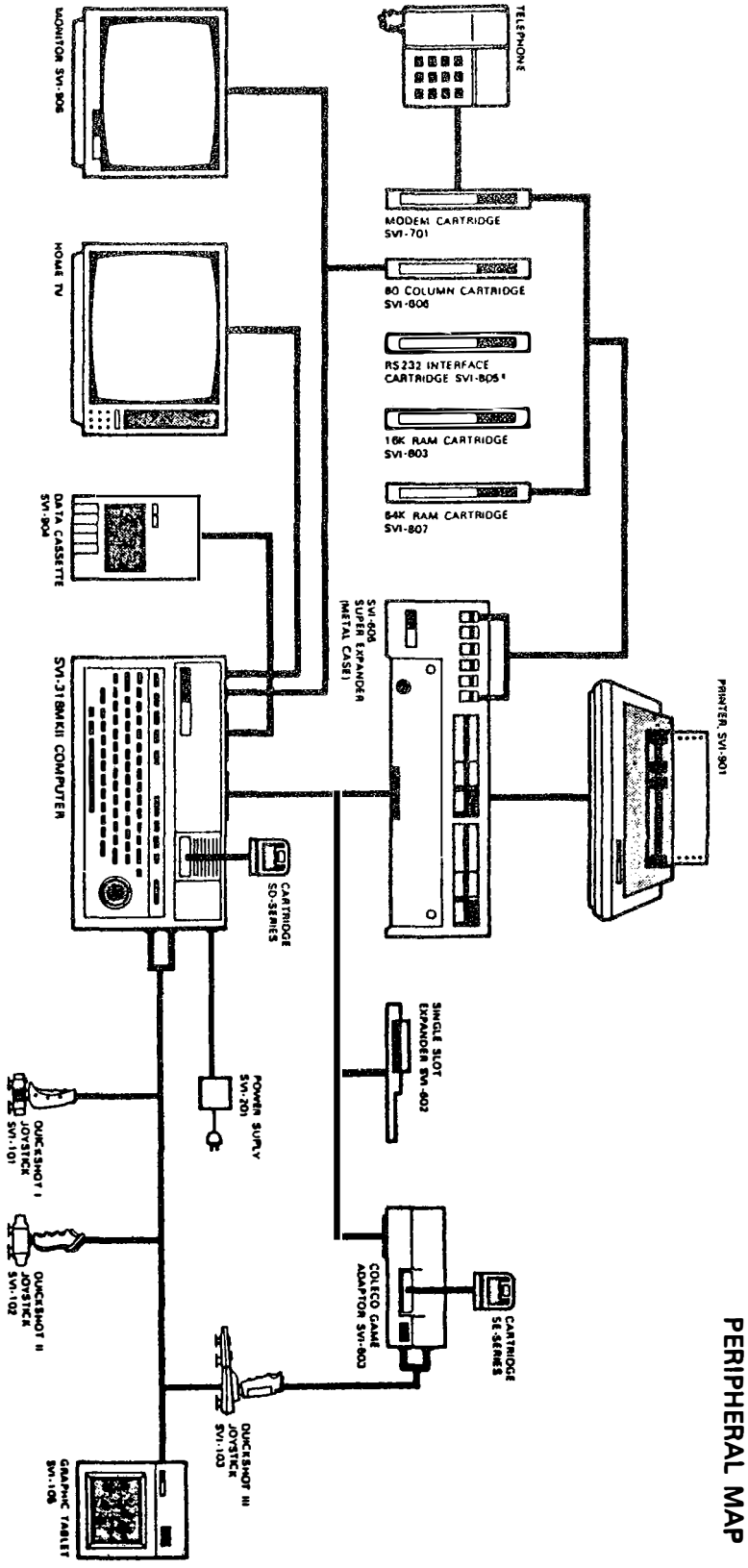


* SVI-318/SVI-328 and Mark II EXPANDER BUS SIGNAL DESCRITPION *

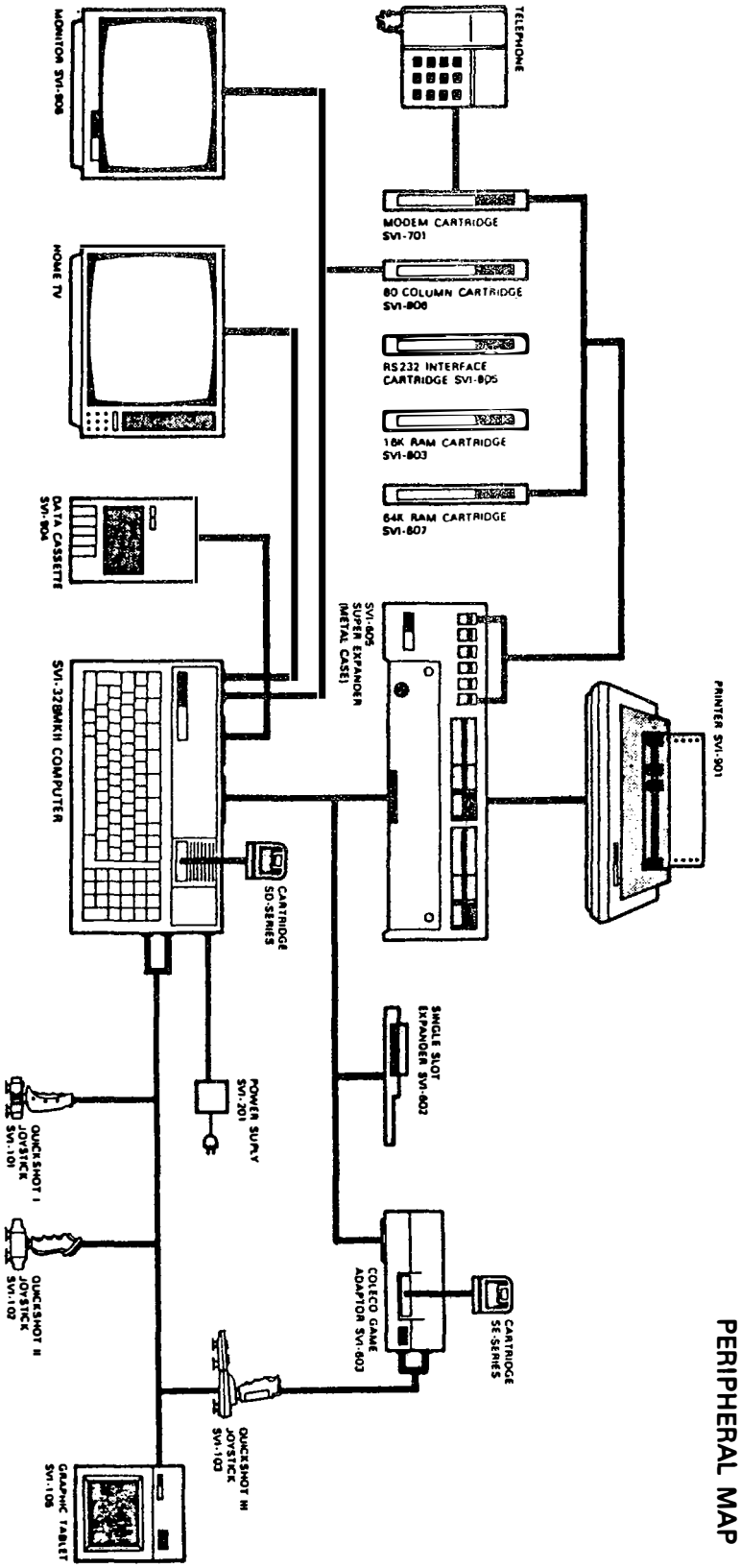
PIN:	NAME:	I/O:	DESCRIPTION:
1	+5V	O	+5V power supply. 300mA current is available for all peripheral cards.
2	$\overline{\text{CNTRL2}}$	I	Spectravideo game adaptor for coleco games CONTROL signal (normally held HIGH by a 3.3K ohm resistor). This signal, when the game adaptor is in use, controls the data transfer between the CPU and the adaptor during the external I/O addressing.
3	+12V	O	+12V power supply. Maximum current is 100mA for all peripheral cards.
4	-12V	O	-12V power supply. Maximum current is 50mA for all peripheral cards.
5	$\overline{\text{CNTRL1}}$	I	Spectravideo game adaptor for coleco games CONTROL signal (normally held HIGH by 1K ohm resistor). This signal, when pulled LOW (i.e. When the adaptor is in use), disables all internal (i.e. SVI-318/SVI-328 and Mark II) I/O address decoding, and inverses A15.
6	$\overline{\text{WAIT}}$	I	Indicates to Z80A CPU that the addressed memory or I/O devices are not ready for data transfer.
7	$\overline{\text{RST}}$	I	When this signal is pulled LOW the CPU begins a RESET cycle. During this RESET cycle, the address and data bus enter a high impendance state and the control signals enter the inactive state.
8	CPUCLK	O	Buffered system clock of frequency 3.58MHz.
9-24	A15-A0		Buffered ADDRESS BUS. This is a 16-bit address bus providing addresses for memory data exchange and I/O device data exchange.
25	$\overline{\text{RFSH}}$	O	Buffered REFRESH signal for the dynamic RAM expanders only. This signal indicates that the lower 7 bits of the address bus contain a refresh address for the dynamic RAM.

PIN:	NAME:	I/O:	DESCRIPTION:
26	$\overline{\text{EXCSR}}$	I	This is the external CPU-from-VDP READ select signal, and is used by Spectravideo game adaptor for coleco$_{TM}$ games.
27	$\overline{\text{M1}}$	O	Buffered MACHINE ONE CYCLE signal. This signal indicates that OP code fetch cycle is the current machine cycle.
28	$\overline{\text{EXCSW}}$	I	This is the external CPU-toVDP WRITE select signal, and is used by Spectravideo game adaptor for coleco games only.
29	$\overline{\text{WR}}$	O	Buffered WRITE signal. This signal indicates that the CPU data bus holds valid data for storage in the addressed memory or I/O device.
30	$\overline{\text{MREQ}}$	O	Buffered MEMORY REQUEST signal. This signal indicates when the address bus is holding a valid memory address.
31	$\overline{\text{IORQ}}$	O	Buffered INPUT/OUTPUT REQUEST signal. This signal indicates the lower 8 bits of the address bus are holding a valid I/O device address, and is at high state (i.e. inactive) during the INTERRUPT cycle.
32	$\overline{\text{RD}}$	O	Buffered READ signal. This signal indicates that the Z80A CPU is wanting to read data from memory or an I/O device.
33-40	D0-D7		Buffered bidirectional DATA bus. This is an 8 bit bidirectional data bus for data exchange between memory and I/O devices.
41	CSOUND	I	Audio input signal from the Spectravideo game adaptor for coleco games.
42	$\overline{\text{INT}}$	I	Generated by I/O devices to request interrupt to Z80A CPU.
43	$\overline{\text{RAMDIS}}$	I	Pulling this signal LOW disables the SVI-318/ SVI-328 and Mark II user RAM. This line is held high by a 1K ohm resistor to +5V.
44	$\overline{\text{ROMDIS}}$	I	Pulling this signal LOW disables the SVI-318/ SVI-328 and Mark II BASIC ROM on board.

PIN:	NAME:	I/O:	DESCRIPTION:
45	$\overline{BK32}$	O	Buffered MEMORY BANK CONTROL signal. Pulling this signal LOW enables the bank 32 portion of the memory (32K, Addr.-- 8000H-FFFFH), and disables the user RAM on board through the $\overline{RAMDIS}$ signal.
46	$\overline{BK31}$	O	Buffered MEMORY BANK CONTROL signal. Pulling this signal LOW enables the bank 31 portion of the memory (32K, Addr.-- 0000H-7FFFH), and disables the BASIC ROM on board through the $\overline{ROMDIS}$ signal.
47	$\overline{BK22}$	O	Buffered MEMORY BANK CONTROL signal. Pulling this signal LOW enables the bank 22 portion of the memory (32K, Addr.--8000H-FFFFH) and disables the usser RAM on board through the $\overline{RA\ DIS}$ signal.
48	$\overline{BK21}$	O	Buffered MEMORY BANK CONTROL signal. Pulling this signal LOW enables the bank 21 portion of the memory (32K, Addr.-- 0000H-7FFFH) which is the lower portion of SVI328 user addressable memory, and disables the BASIC ROM on board.
49-50	GND		System electrical ground.

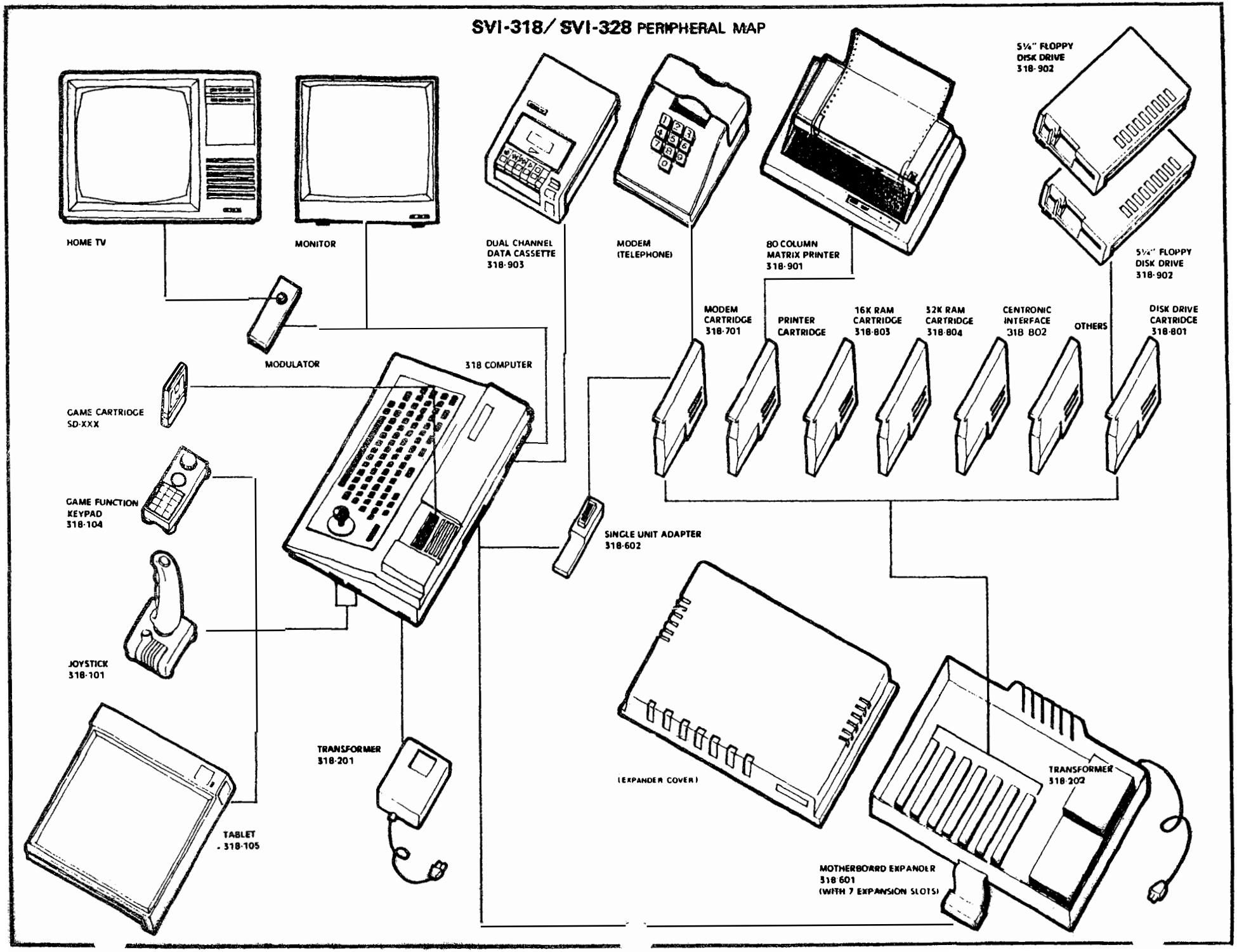


THE SVI-318MKII SYSTEM
PERIPHERAL MAP



THE SVI-328MKII SYSTEM
PERIPHERAL MAP

SVI-318/ SVI-328 PERIPHERAL MAP



3. DIAGNOSTIC TEST AND TROUBLE SHOOTING CHART

A cartridge is available to test the SVI-318/SVI-328 computer hardware:

1. CPU and OUTPUT BUFFERS to the EXPANDER
2. USER RAM
3. VIDEO RAM (VRAM)
4. PROGRAMMABLE SOUND GENERATOR (PSG)
5. SOUND CHANNEL
6. VDP INTERRUPT
7. CASSETTE LINE (CASW/CASR, ME/RE)
8. KEYBOARD LINE (OUTPUT/INPUT)
9. JOYSTICK 1 AND 2

Using the Test Programme

1. To use the testing programme, be sure the power is off, plug the cartridge into the GAME CARTRIDGE SOCKET, the keyboard and the cassette interface into the socket, and then switch on.

   The programme will print the below message:

   ** SVI-318 COMPUTER TESTING RESULT **

   If the printer fails to print the message, it indicates that errors may occur in any one of the followings:

   i) CPU
   ii) OUTPUT BUFFERS
   iii) USER RAM

2. If no errors occur in the testing of the USER RAM, the message 'USER RAM OK' is printed. However, if an error does occur, the message 'USER RAM ERROR' is printed and the following information will be given:

ADDRESS: XXXX	address of the memory location at which an error is found.
DATA WRITE: YY	data written to addressed location.
DATA READ: ZZ	data read from the addressed location.

   Test pattern set written to the memory is 00,01,02,.....FC,FD,FE.

3. If no errors are found in the testing of the VRAM, the message 'VRAM OK' is printed. However, if an error does occur, the message 'VRAM ERROR' is printed, and the following information will be given:

ADDRESS: XXXX	address of the memory location at which an error is found.
DATA WRITE: YY	data written to the location addressed by the above address.
DATA WRITE: YY	data read from the location addressed by the above address.

Test pattern set: 00,01,02,.....FC,FD,FE.

4. If no errors occur in the testing of PSG, the message 'PSG OK' is given, and followed by three tones. However, if 'PSG ERROR' is given, it means that the PSG chip is not functioning property.

5. Sound Channel is on for few seconds (no listing given in this stage).

6. VDP INTERRUPT testing:

VDP INTERRUPT OK	VDP chip functions properly.
VDP INTERRUPT ERROR	VDP chip is not functioning properly.

7. CASSETTE LINE testing:

If there is no error, "CASSETTE LINE OK" message is printed, otherwise "CASSETTE LINE ERROR" message is printed to indicate CASSETTE LINE is not functioning properly.

There are our ways to test CASSETTE LINE, the procedures are as follows:

(a) input CASW=0 (low), output CASR=1 (high), if not, "ERROR, TEST 1----CASW/CASR" message is printed input ME=0 (low), output RE=1 (high),

if not, "ERROR, TEST 1----ME/RE" message is printed.

(b) input CASW=0 (low), output CASR=1 (high), if not, "ERROR, TEST 2----CASW/CASR" is printed input ME=1 (high), output RE=0 (low), if not, "ERROR, TEST 2----ME/RE" is printed.

(c) input CASW=1 (high), output CASR=0 (low), if not, "ERROR TEST 3----CASW/CASR" is printed input RE=0 (low), output ME=1 (high), if not, "ERROR TEST 3----ME/RE" is printed.

(d) input CASW=1 (high), output CASR=0 (low), if not "ERROR, TEST 4----CASW/CASR" is printed input ME=1 (high), output RE=0 (low), if not, "ERROR, TEST 4----ME/RE" is printed. A "CASSETTE LINE TESTING COMPLETED" is printed at the end of the test, this message is printed when error occurred only.

8. KEYBOARD LINE testing:

If there is no error, "KEYBOARD LINE OK" message is printed, otherwise "KEYBOARD LINE ERROR" message is printed to indicate the KEYBOARD LINE is not functioning properly.

This test is checking all 10 outputs and 8 inputs, each output and input are corresponded, a message will print to indicate which corresponding output/input line has error.

The error message for corresponding output/input line as follow:

(1) "ERROR OUTPUT 0/INPUT 2"
(2) "ERROR OUTPUT 1/INPUT 1"
(3) "ERROR OUTPUT 2/INPUT 7"
(4) "ERROR OUTPUT 3/INPUT 6"
(5) "ERROR OUTPUT 5/INPUT 6"
(6) "ERROR OUTPUT 6/INPUT 5"
(7) "ERROR OUTPUT 7/INPUT 0"
(8) "ERROR OUTPUT 8/INPUT 4"
(9) "ERROR OUTPUT 9/INPUT 5"
(10) "ERROR OUTPUT 10/INPUT 7"

All output=0 (low), input 1 (high)

A "KEYBOARD LINE TESTING COMPLETED" message is printed at the end when errors occur only.

9. JOYSTICK testing:

JOYSTICK 1---) GREEN CURSOR
JOYSTICK 2---) RED CURSOR

If error in (7), (8) and (9), check PSG and PPI.

10. In CP/M 2.22 version system disk enclosed memtst. com memory test in CP/M mode

BIOS located at E600
which starts above this programme and ends at BIOS.

Starting address (HEX) 09BB
Ending address (HEX) E5Ff

(1) Bit stuck high or low test
(2) Adjacent bits shorted test
(3) Checksum (55AAH pattern) test
(4) Walking bit left test
(5) Walking bit right test
(6) Address line test
(7) Random number test cycle: 1,2,3,4,5,6,7,8
(8) MI cycle test - 4K block:

SA200 MAINTENANCE EQUIPMENT

Alignment Diskette

The SA124 alignment diskette is used for alignment of the SA200. The following adjustments and checks can be made using the SA124.

a. Read/Write head radial adjustment using track 16.

b. Index Photo detector alignment using track 01.

c. Track 00 is recorded with a 125 kHz signal (2F). This track is used to designate if the head is positioned over track 00 when the track 00 indication is true.

d. Track 34 has a 125 kHz signal (2F) recorded, and specifies if the head is positioned over track 34. It is also used for reference purposes.

Caution should be exercised not to destroy pre-recorded alignment tracks. These tracks are: 00, 01, 15, 16, 17 and 34. The write protect tab should always be installed on the SA124 to prevent accidental writing on the diskette.

Exerciser

The exerciser used on the SA200 consists of an 809 exerciser with a special cable set. This exercise PCB can be used in a stand alone mode, built into a test station, or used in a tester for field service.

The exerciser enables the user to perform all adjustments and checks required on the SA200 drive. It has no intelligent data handling capabilities but can write a 2F 125 kHz signal which is the recording frequency used for amplitude checks on the SA200. The exerciser can also start and stop the drive motor, and enables read in the SA200 to allow checking of proper read back signals.

DIAGNOSTIC

Introduction

Incorrect operating procedures, faulty programming, damaged diskettes, "soft errors" created by airbome contaminants, and other external causes can produce errors falsely attributed to drive failure or misadjustment. Unless visual inspection of the drive discloses an obvious misalignment or broken part, attempt to repeat the fault with the original diskette, then attempt to duplicate the fault on a second diskette.

"Soft Error" Detection and Correction

Soft errors are usually caused by:

a. Airborne contaminants that pass between the read/write head and the disk. Usually, these contaminants can be removed by the cartridge self-cleaning wiper.

b. Random electrical noise that usually lasts for a few microseconds.

c. Small defects in the written data and/or track not detected during the write operation that may cause a soft error during a read.

d. Worn or defective load pad.

e. Improper grounding of the power supply, drive, and/or host system.

f. Improper motor speed.

The following procedures are recommended to recover from the above mentioned soft errors:

a. Re-read the track ten times or until data is recovered.

b. If data is not recovered after performing step (a), access head to adjacent track in same direction previously moved, then return to desired track.

c. Repeat step (a).

d. If data is not recovered, error is not recoverable.

Write Error

If an error occurs during a write operation, it will be detected on the next revolution by doing a read operation, commonly called a "write check." To correct the error, another write and check operation must be done. If the write operation is not successful after ten attempts, a read operation should be attempted on another track to determine whether the media or the drive is failing. If the error still persists, the diskette should be replaced and the above procedure repeated. If the failure still exists, consider the drive defective. If the failure disappears, consider the original diskette defective and discard it.

Read Error

Most errors that occur will be "soft errors." In these cases, performing an error recovery procedure will recover the data.

Seek Error

a. Stepper malfunction

b. Carriage binds.

c. To recover from a seek error, recalibrate to track 00 and perform another seek to the original track. Another alternative is to perform a read I.D. to determine on which track the head is located and compensate accordingly.

Equipment Set-Up

Connect the power supply and modulator to the computer and the TV receiver (select the right channel and the TV-System). Turn on the lower switch, the "POWER ON" LED should light up and "SPECTRAVIDEO" logo prompt on the screen and changing colour three times.

Basic Functional Check

1. Type the following programme:

   10 FOR X = 1 to 254

   20 ? CHR $ (X);: NEXT: GOTO 10

   (Press 'ENTER' in each statement)

2. Press "F5" (To run the programme)

3. Observe that all characters and graphic symbols will be displayed repeatedly. Perform shock test during the programme is running and make sure the programme will not be interrupted or terminated by the shock in the test.

4. Press "STOP", observe that programme is temporary stopped by this. Press "STOP" again and note that the programme will continue.

5. Press "CRTL STOP", the programme should terminated by this command and the "OK" prompt reappear.

6. Press "F4" (List the programme) and observe the programme content is listed out without error.

7. Move the cursor within a line and then press "INS/PASTE", type in several characters and observe that the characters are inserted.

8. Press "DEL/CUT" to delete the character under the cursor.

9. Press "CLS/HM" and observe that the screen should be clear and the cursor appear at the left-top position.

10. Press "F4" and observe the programme content is listed out.

11. Type "NEW" and presss "ENTER", the press "F4" again to confirm the programme is cleared from the memory.

12. Press each key to check that the characters are correctly displayed.

13. Press "CAP LOCK" and then press several keys to check the capital letters are printed.

14. Press "SHIFT" and then simultaneously press several keys to check the capital letters are printed.

15. Press "LEFT GRPH"/"RIGH GRPH" and then simultaneously press several keys to check the graphic symbols are displayed.

16. Turn the power off.

Diagnostic Test

1. Connect the super expander SVI-601 to the computer.

2. Insert the printer interface SVI-802 cartridge in any one of the slots except slot 6.

3. Connect the printer SVI-901 to the printer interface through a flat cable.

4. Insert the "Tester" cartridge into the cartridge slot of the computer.

5. Turn the power on.

6. Observe that the following message should be printed from the printer.

   SVI-318 computer testing result:

   User RAM OK

   VRAM OK

   PSG OK

   VDP INT OK (after three tones from the TV)

7. Three cross-marked colour cursors should be appeared on the TV screen. Connect the joystick to socket connector 1 in the right hand side of the unit.

8. Move the joystick in different directions and make sure that the cursor follows the same motion.

9. Press the fire button on the joystick and an explosive sound should be heard.

10. Repeat step 8 to 9 for joystick socket connector 2 and the built-in joystick pad.

11. Press each key in the keyboard and a continuous tone should be heard.

12. Turn the computer off.

Cassette Interface Test

1. Connect the data cassette SVI-903 to the computer through the cassette interface socket at the back.

2. Turn on the power.

3. Type "SOUND ON" and press "ENTER".

4. Insert a "Colour Pattern" tape into the cassette.

5. Type "CLOAD" and press "ENTER".

6. Press "PLAY" button on the cassette.

7. The programme in the tape is being loaded into the computer. Press "STOP" button on the cassette after "OK" reappeared.

8. Type "CSAVE "BAR"" and press "ENTER".

9. Press 'PLAY and RECORD' buttons simultaneously on the cassette as directed from the computer.

10. Press "Stop" button after an "OK" appeared on the screen.

11. Type "NEW" and press "ENTER".

12. Rewind the tape in the cassette.

13. Type "CLOAD "BAR"" and press "ENTER"

14. Press the "PLAY" button on the cassette after the "FOUND:BAR" and 'OK' appeared on the screen.

15. Press "STOP" button on the cassette after the "FOUND:BAR" and 'OK' appeared on the screen.

16. Press "F5" to run the programme.

17. A colour pattern with music notes will be observed, press "CRTL STOP" to stop the programme.

18. Type "LLIST" and press "ENTER", then the programme will be listed from the printer.

19. Turn off the power.

Disk Basic Test

1. Insert the disk controller cartridge SVI-801 to the slot SK6 in the super expander.

2. Connect 2-disk drive SVI-902 to the disk controller through the flat cables.

3. Insert the BASIC disk to the disk drive A.

4. Turn the disk lock to vertical position and turn on the power in computer.

5. Type "FILES" and press "ENTER".

6. Type "RUN"1: NOMIS"" and press "ENTER".

7. Observe that the programme "NOMIS" will execute without problem.

8. Press "CRTL STOP" to terminate the programme.

9. Type "NEW" and press "ENTER" to clear the memory.

10. Type the following programme:

    10 SCREEN 1

    20 CIRCLE (128, 96), 80, 11

    30 PAINT (128, 96), 11

    40 GOTO 40

    (Press "ENTER" after each statement)

11. Type "SAVE"1:CIR"" and press "ENTER".

12. After the screen shows "OK", type "FILES" and press "ENTER", the "CIR" file should be included in the list.

13. Type "LOAD"1: CIR"" and press "ENTER", wait until the computer prints "OK".

14. Press "F5". (Run the programme)

15. Press "CRTL STOP" to stop the programme.

16. Type "NEW" and press "ENTER" to clear the memory.

17. Type "KILL"1:CIR"" and press "ENTER" to erase the file "CIR", wait until the computer print "OK".

18. Type "FILES" and press "ENTER", observe that the file "CIR" should disappear.

19. Turn off the power.

CP/M Disk Test

1. Insert the 64K RAM cartridge into any slots of SVI-601 super expander except SK6. Set the switch BK21 and 02 ON. (Delete this step for SVI-328).

2. Insert the CP/M disk to the disk drive A and the copy disk (Blank disk) to the disk drive B.

3. Lock the doors in both drives and turn on the power in computer.

4. Wait until "A " shown on the screen.

5. Type "DIR" and press "ENTER", the directory list should be appeared on the screen.

6. Type "DDT" and press "ENTER", 'DDT VERS 2.2' is shown.

7. Type "L" and press "ENTER". (Repeat this step six times)

8. Type "D" and press "ENTER". (Repeat this step three times)

9. In both cases, a message of machine language should be observed.

10. Press "CRTL C" to stop the programme.

11. Type "SVFORMAT" and press "ENTER".

12. Type "B" to format the diskette in drive B and press "ENTER".

13. Wait until "verifying track 39" is shown on the screen.

14. Type "N" and press "ENTER", wait until command 'A ' reappear on the screen.

15. Type "DIR B:" and press "ENTER" to list the directory in the copy diskette in drive B to confirm that the copying is completed.

16. Type "ERASE B:*.*" and press "ENTER" to erase the files in the diskette in drive B.

17. Type "Y" and press "ENTER" to confirm and wait until command 'A ' reappear on the screen.

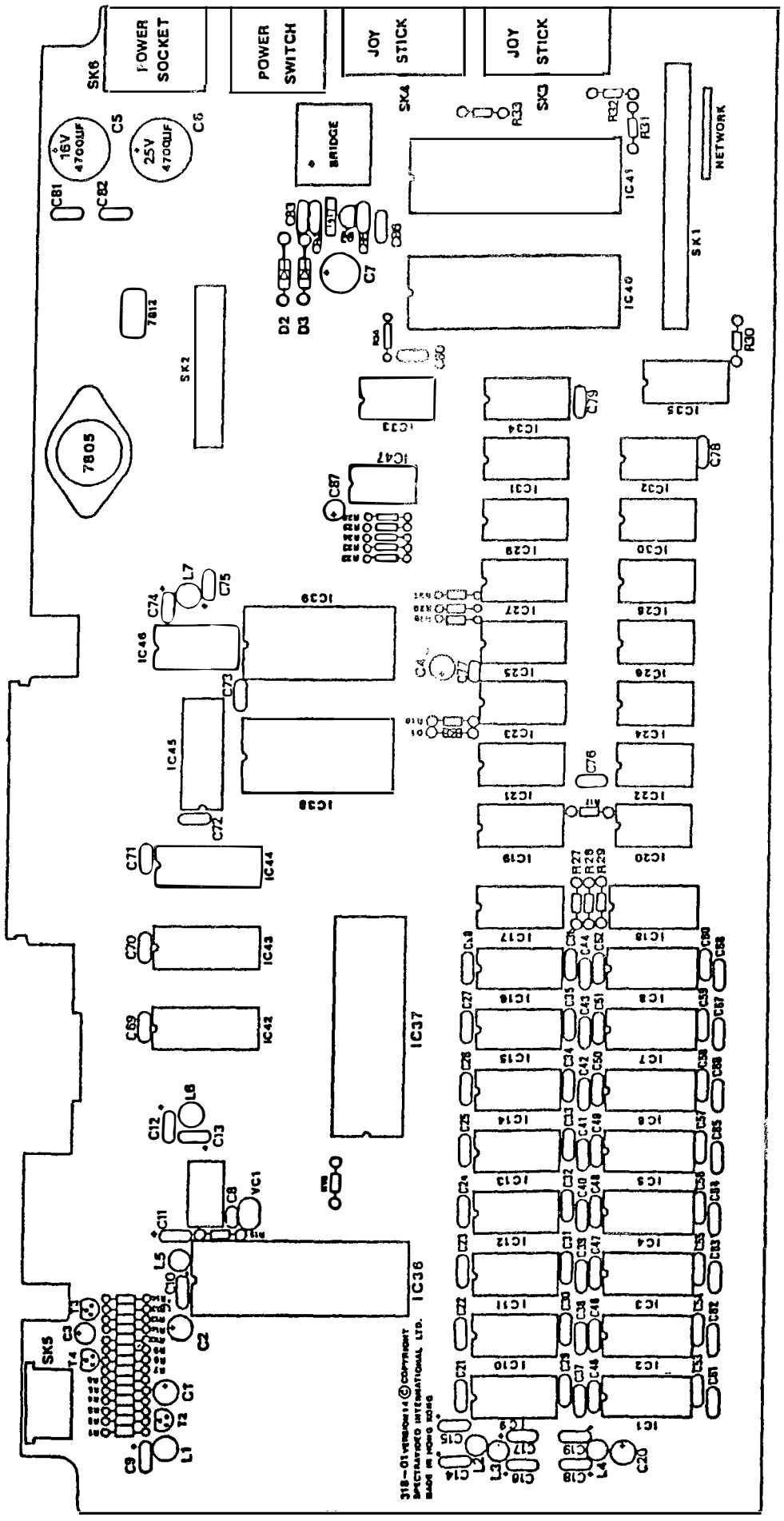
18. Type "DIR B:" and press "ENTER". Note that "No Files" should be observed to show that the erase is OK.

19. Turn off the power.

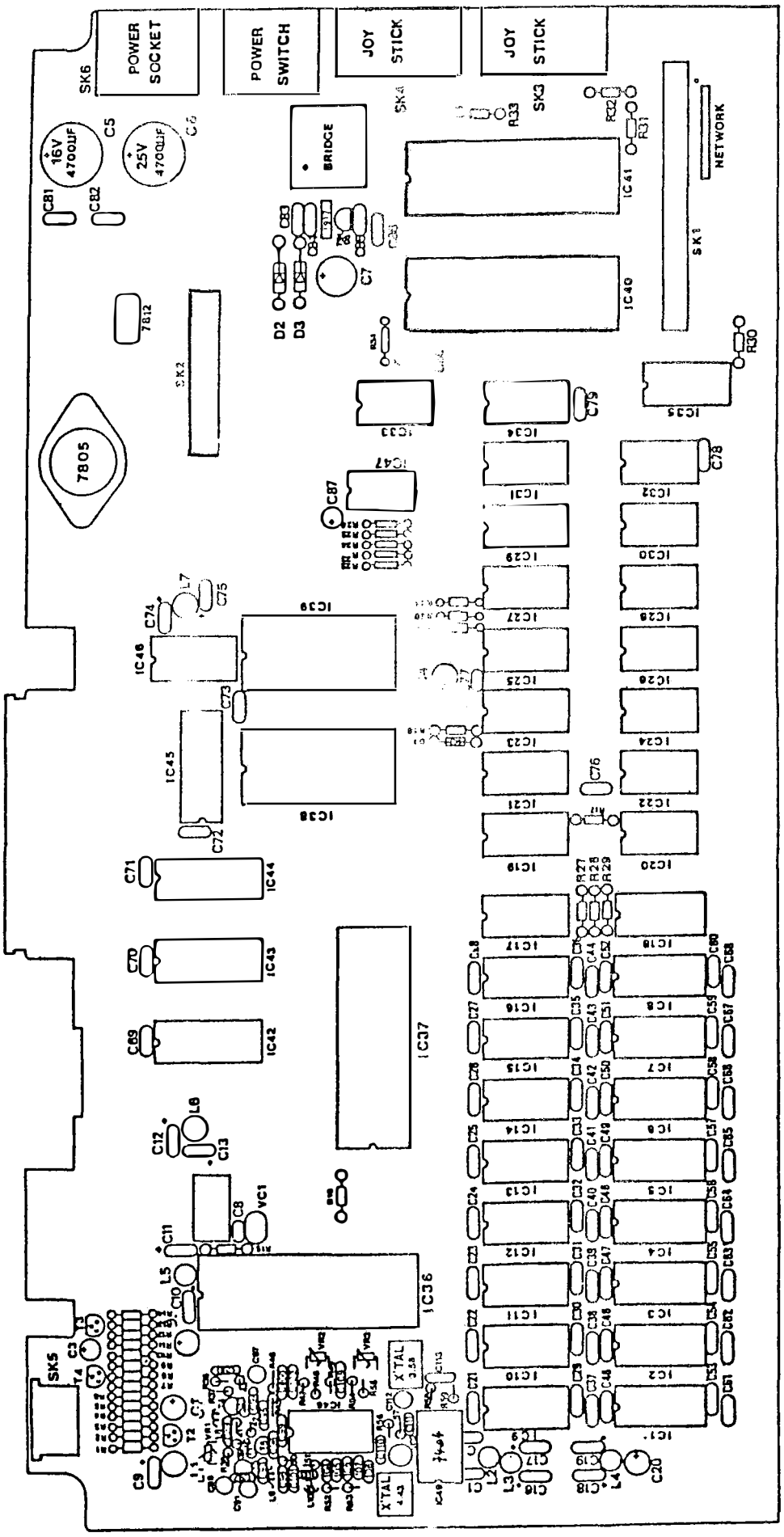
TROUBLE SHOOTING CHART

SYMPTON	POSSIBLE CAUSE	REMEDY
No power	Power switch not turned on	Turn on power switch which is on right-hand side of the machine.
	Power cable not connected	Be sure the power cable is connected to the computer and replace the brown fuse.
No sound or picture	Wrong TV channel	Select correct TV channel.
	Loose video cable	Be sure all video cables are securely fastened.
	TV volumn and colour too low	Adjust TV the volumn control and colour level of your TV.
	No master clock	Use oscilloscope to check IC23 pin 4 and IC36 Pin 39.
No picture	+5V	C8 and 7805C pin 2
	+12V	C114 and 7812C pin 3
	-12V	7912C pin 3 or 79L05 pin 2
	-5V	79L05 pin 3 and C85
	$\overline{\text{RESET}}$	IC37 pin 26
No function	No master clock	IC36 pin 39, 38 and IC37 pin 6
	Interrupt	IC37 pin 17, 16, 19 and 20
		IC36 pin 16
	ROM chip select	IC31 pin 11, 12
	User RAM chip select	IC1 - 8 and IC17, 18, pin 3, 4, 15
No picture or sound	Wrong TV channel	Select correct TV channel
	Loose video cable	Be sure all video cable are securely fastened
	VRAM chip select	IC9 - 16, pin 3, 4, 15
	VDP interrupt	IC36, pin 16

SVI-318/328 NTSC VERSION



SVI-318/328 PAL VERSION



```
10 REM   Memory bank ram size test program
20 REM   Make sure you have 64K ram card
30 REM   One have BK21 on, the other have BK31 on, (in 32K option)
31 REM
40 CLEAR 10,&HD000
50 '
60 B2=&HD042:B3=&HD044
70 FOR K=&HD000 TO B3
80 READ A$:POKE K,VAL("&H"+A$)
90 NEXT K
100 DEF USR2=&HD011 'TEST BK 21
110 DEF USR3=&HD02B 'TEST BK 31
120 '---- INIT RAM AREA ----
130 FOR I=B2 TO B3+1
140 POKE I,0
150 NEXT I
160 A=USR3(0)
170 A=USR2(0)
180 PRINT"BANK 21 =";256*(PEEK(B2+1))+PEEK(B2)
190 PRINT"BANK 31 =";256*(PEEK(B3+1))+PEEK(B3)
200 STOP
210 REM --- DATA ----
220 DATA 21,00,00 :REM 'CHKSIZ: LD HL,0 ;0-7FFFH
230 DATA 7E       :REM '      CPL
250 DATA 2F       :REM '      LD (HL),A ;WRITE
260 DATA BE       :REM '      CP (HL)
270 DATA 2F       :REM '      CPL
280 DATA 77       :REM '      LD (HL),A ;SAVE BACK
290 DATA C0       :REM '      RET NZ
300 DATA 23       :REM '      INC HL
310 DATA 7C       :REM '      LD A,H    ;EXIT FOR HL=8000
320 DATA FE,80    :REM '      CP 80H
330 DATA 20,F3    :REM '      JR NZ,CHKSZ1
340 DATA C9       :REM '      RET       ;HL=SIZE
350 '
360 ' PSG,PORTB: ROMEN1,ROMEN0,CAP,BK32,BK31,BK22,BK21,CART
370 '              D7     D6    D5  D4   D3   D2   D1   D0
380 ' IN PSG DATA : 90H
390 ' OUT PSG DATA: 8CH
400 ' OUT PSG LATCH: 88H
410 '
420 DATA F3       :REM 'CHK21: DI
430 DATA 3E,0F    :REM '       LD A,0FH        :PORT B
440 DATA D3,88    :REM '       OUT (88H),A     ; LATCH
450 DATA DB,90    :REM '       IN A,(90H)      ; CURRENT BANK COND
460 DATA 47       :REM '       LD B,A          ; B=OLD BANK COND
470 DATA E6,FD    :REM '       AND 11111101B   ; BANK 21 ON
480 DATA D3,8C    :REM '       OUT (8CH),A
490 DATA 21,00,00 :REM '       LD HL,0000      ; no meaning
500 DATA CD,00,D0 :REM '       CALL CHKSIZ     ; RESULT IN HL
```

```
510 DATA 22,42,DO :REM '       LD (BK21),HL     ; SAVE RAM SIZE
520 DATA 78       :REM '       LD A,B-          ; A = ORG BANK COND
530 DATA D3,8C    :REM '       OUT (8CH),A
540 DATA FB       :REM '       EI
550 DATA C9       :REM '       RET
560
570 DATA F3       :REM 'CHK31: DI
580 DATA 3E,OF    :REM '       LD A,OFH         ; PORT
590 DATA D3,88    :REM '       OUT (88H)        ; LATCH
600 DATA DB,90    :REM '       IN A,(9OH)
610 DATA 47       :REM '       LD B,A
620 DATA E6,F7    :REM '       AND 11110111B    ; BANK 31 ON
630 DATA D3,8C    :REM '       OUT (8CH),A      ;
640 DATA CD,OO,DO :REM '       CALL CHKSIZ      ; RESULT IN HL
650 DATA 22,44,DO :REM '       LD (BK31),HL     ; DATA SAVE
660 DATA 78       :REM '       LD A,B           ; ORG BANK COND
670 DATA D3,8C    :REM '       OUT (8CH),A
680 DATA FB       :REM '       EI
690 DATA C9       :REM '       RET
700 DATA OO,OO    :REM '       BK21: DS 2       ; MEMORY SIZE OF BANK 21
710 DATA OO,OO    :REM '       BK22: DS 2       ; MEMORY SIZE OF BANK 31
720 FOR I=&HKOOO TO B3+1
730 LPRINTHEX$(I);" ";HEX$(PEEK(I))
740 NEXT
```

```
10  SCREEN 1
20  FOR I=0 TO 20
30  CIRCLE (128,96),I*5
40  NEXT I
50  LINE (0,0)-(255,191),,B
60  LINE (0,0)-(255,191);LINE(255,0)-(0,191)
70  '
80  '
90  '----------- check & plot -----
100 FOR Y=0 TO 192 STEP 7
110       LPRINT CHR$(8);
120       FOR X=0 TO 255
130       '
140       A=&H80
150       FOR B=0 TO 6       ' PLOT 7 DOTS
160       A=A+ABS(POINT(X,Y+B)=15)*2 (B)
170       NEXT B
190       LPRINT CHR$(A);    'PRINT 1 BYTE BIT PATTERN
210       NEXT X
220                 LPRINT CHR$(&HA);  'NEXT LINE
230       NEXT Y
```

4. THEORY OF OPERATION DESCRIPTION

SYSTEM ARCHITECTURE

The Spectravideo SVI-318/SVI-328 and MarK II home computer is a computational tool based on a Zilog 80A microcomputer system Figure 4-1. The Zilog 80A microprocessor unit (μP) provides control logic, data manipulation and computation capability to the SVI-318/SVI-328 and Mark II home computer. The μP uses contents of read-only memory (ROM) to specify how the computer is to perform. An Micro-Soft Basic computer language interpreter is implemented as code stored in the system ROM devices. Temporary data and results of computations can be stored in random-access memory (RAM). Data in RAM can also be μP instructions, but is more often Basic language programme instructions and computational data.

Bit patterns in ROM specify the type of activity to be performed by the μP. These instructions (bit patterns) cause various operations to be performed.

(1) Read the data at a specified address location and place it in an μP register.

(2) Write the data from an μP register to a specified addressable location may be RAM, VDP, PPI or PSG.

(3) Perform computational or data comparison procedures on specified data.

(4) Jump or branch to a location other than the next successive memory location to retrieve the next instruction for programme execution. These jump or branch operations are often determined by interrogating the result or status of an arithmetic or logical computational operation.

(5) Stop and wait for interrupt.

(6) Branch to and return from subroutines.

(7) Branch to a vectored routine to service interrupts and system restart operations.

The Zilog 80A μP uses a 64K address space. The lower 32K is dedicated for ROM device and peripheral interface devices such as PIO and VDP. The upper 32K is dedicated for RAM devices (8000H - FFFFH in hexadecimal notation).

The various elements that share the 64K address space possess unique attributes.

CPU ARCHITECTURE

A block diagram of the internal architecture of the Z-80 CPU is shown in Figure 4-2. The diagram shows all of the major elements in the CPU and it should be referred to throughout the following description.

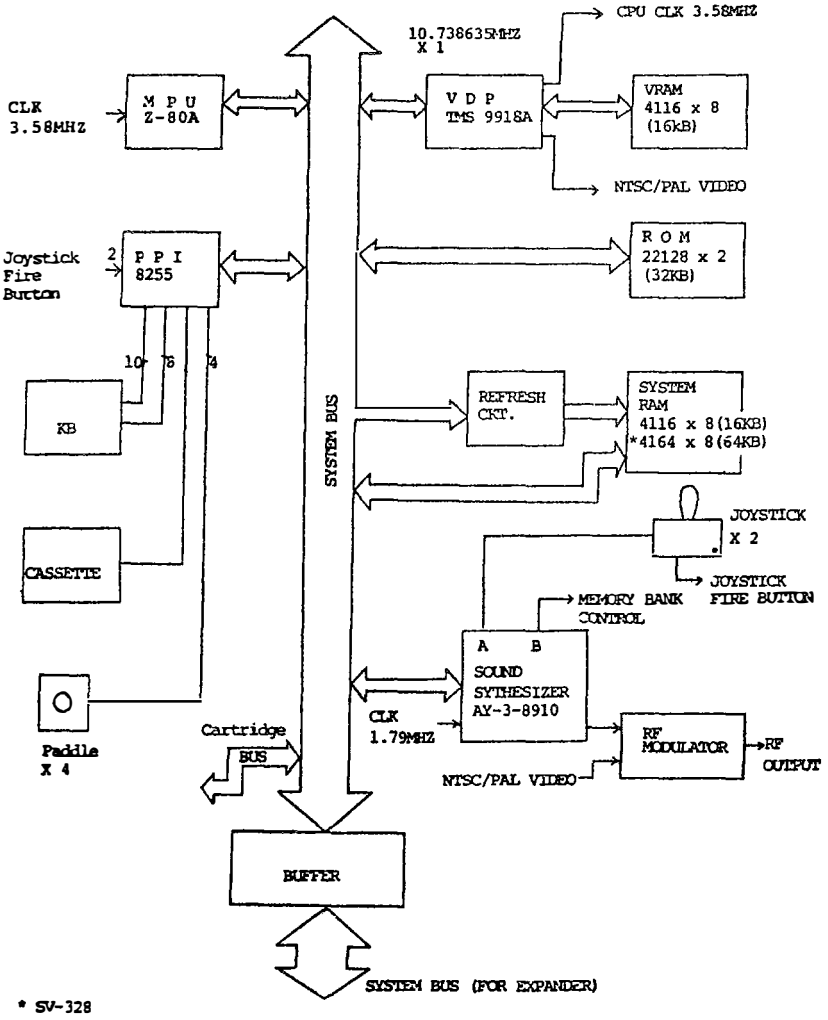


FIG. 4-1

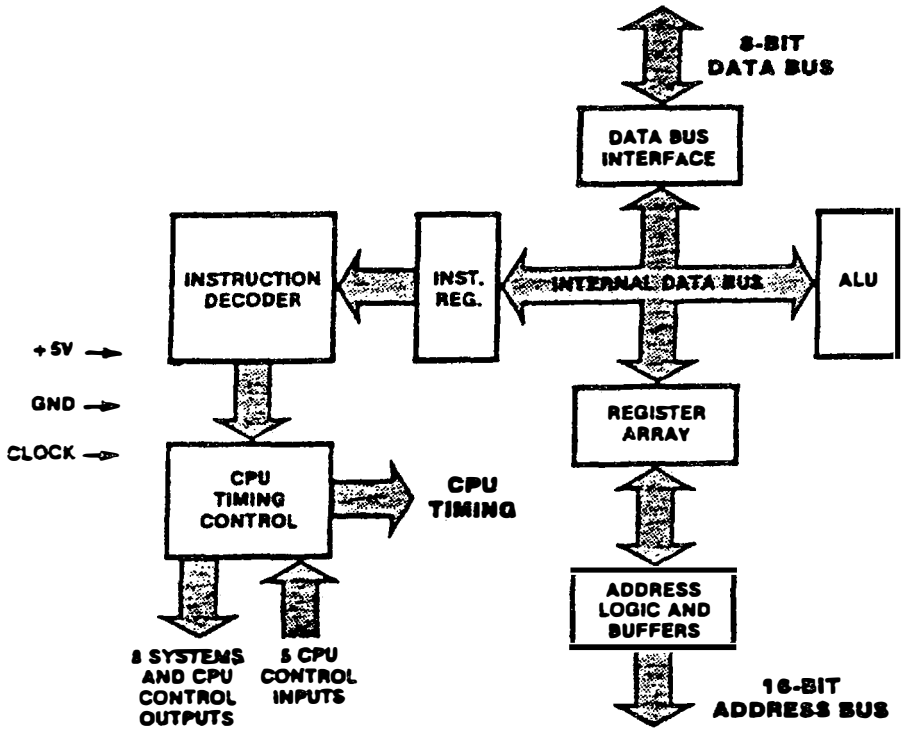


FIG. 4-2 **Z80CPU Block Diagram**

CPU RESGISTERS

The Z-80 CPU contains 208 bits of R/W memory that are accessable to the programmer. Figure 4-3 illustrates how this memory is configured into eighteen 8-bit regters and four 16-bit registers. All Z-80 registers are implemented using static RAM. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or in pairs as 16-bit registers. There are also two sets of accumulator and flag registers.

SPECIAL PURPOSE REGISTERS

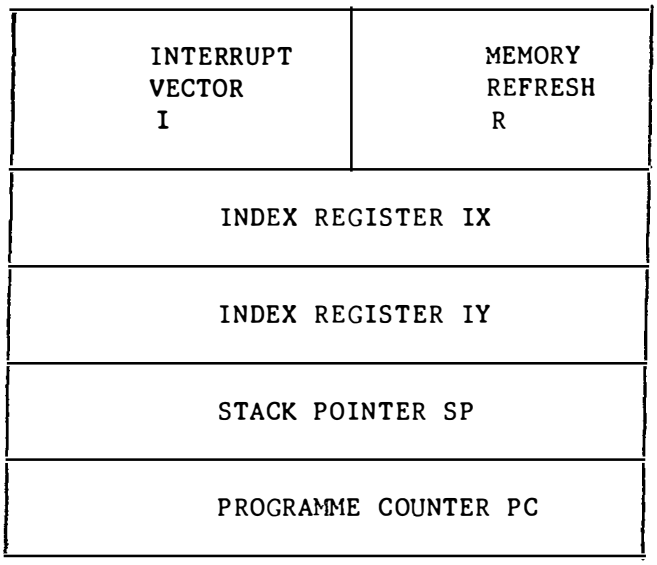
(1) Programme Counter (PC).

The programme counter holds the 16-bit address of the current instruction being fetched from memory. The PC is automatically incremented after its contents have been transferred to the address lines. When a programme jump occurs the new value is automatically placed in the PC, overriding the incrementer.

(2) Stack Pointer (SP).

The stack pointer holds the 16-bit address of the current top of a stack located anywhere in external system RAM memory. The external stack memory is origanized as a last-in first-out (LIFO) file. Data can be pushed onto the stack from specific CPU registers or popped off of the stack into specific CPU registers through the execution of PUSH and POP instructions. The data popped from the stack is always the last data pushed onto it. The stack allows simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data manipulation.

MAIN REG SET		ALTERNATE REG SET		
ACCUMULATOR A	FLAGS F	ACCUMULATOR A'	FLAGS F'	
B	C	B'	C'	GENERAL PURPOSE REGISTER
D	E	D'	E'	
H	L	H'	L'	



Z-80 CPU REGISTER CONFIGURATION

Fig. 4-3

(3) Two Index Registers (IX and IY).

The two independent index registers hold a 16-bit base address that is used in indexed addressing modes. In this mode, an index register is used as a base to point to a region in memory from which data is to be stored or retrieved. An additional byte is included in indexed instructions to specify a displacement is specified as a two's complement signed integer. This mode of addressing greatly simplifies many types of programmes, especially where tables of data are used.

(4) Interrupt Page Address Register (I).

The Z-80 CPU can be operated in a mode where an indirect call to any memory location can be achieved in response to an interrupt. The I Register is used for this purpose to store the high order 8-bits of the indirect address while the interrupting device provides the lower 8-bits of the address. This feature allows interrupt routines to be dynamically located anywhere in memory with absolute minimal access time to the routine.

(5) Memory Refresh Register (R).

The Z-80 CPU contains a memory refresh counter to enable dynamic memories to be used with the same ease as static memories. Seven bits of this 8-bit register are automatically incremented after each instruction fetch. The eighth bit will remain as programmed as the result of an LD R, A instruction. The data in the refresh counter is sent out on the lower portion of the address bus along with a refresh control signal while the CPU is decoding and executing the fetched instruction. This mode of refresh is totally transparent to the programmer and does not slow down the CPU operation. The programmer can load the R register for testing purposes, but this register is normally not used by the programmer. During refresh, the contents of the I register are placed on the upper 8 bits of the address bus.

ACCUMULATOR AND FLAG REGISTERS

The CPU includes two independent 8-bit accumulators and associated 8-bit flag registers. The accumulator holds the results of 8-bit arithmetic or logical operations while the flag register indicates specific conditions for 8 or 16-bit operations, such as indicating whether or not the result of an operation is equal to zero. The programmer selects the accumulator and flag pair that he wishes to work with a single exchange instruction so that he may easily work with either pair.

GENERAL PURPOSE REGISTERS

There are two matched sets of general purpose registers, each set containing six 8-bit registers that may be used individually as 8-bit registers or as 16-bit register pairs by the programmer. One set is called BC, DE and HL while the complementary set is called BC', DE' and HL'. At any one time the programmer can select either set of registers to work with through a single exchange command for the entire set. In systems where fast interrupt response is required, one set of general purpose registers and an accumulator/flag register may be reserved for handling this very fast routine. Only a simple exchange commandss need be executed to go between the routines. This greatly reduces interrupt service time by eliminating the requirement for saving and retrieving register contents in the external stack during interrupt or subroutine processing. These general purpose registers are used for a wide range of applications by the programmer. They also simplify programming, especially in ROM based systems where little external read/write memory is available.

ARITHMETIC AND LOGIC UNIT (ALU)

The 8-bit arithmetic and logical instruction of the CPU are executed in the ALU. Internally the ALU communicates with the registers and the external data bus on the internal data bus. The type of functions performed by the ALU include:

Add	Left or right shifts or rotates (arithmetic and logical)
Subtract	Increment
Logical AND	Decrement
Logical OR	Set bit
Logical Exclusive OR	Reset bit
Compare	Test bit

INSTRUCTION REGISTERS AND CPU CONTROL

As each instruction is fetched from memory, it is placed in the instruction register and decoded. The control sections performs this function and then generates and supplies all of the control signals necessary to read or write data from or to the registers, control the ALU and provide all required external control signals.

Instruction Set

The Z80 microprocessor has one of the most powerful and versatile instruction sets available in any 8-bit microprocessor. It includes such unique operations as a block move for fast, efficient data transfers within memory or between memory and I/O. It also allows operations on any bit in any location in memory.

The instructions are divided into the following categories:

- 8-bit loads
- 16-bit loads
- Exchanges, block transfers, and searches
- 8-bit arithmetic and logic operations
- General-purpose arithmetic and CPU control
- 16-bit arithmetic operations
- Rotates and shifts
- Bit set, reset, and test operations
- Jumps
- Calls, returns, and restarts
- Input and output operations

A variety of addressing modes are implemented to permit efficient and fast data transfer between various registers, memory locations, and input/output devices. These addressing modes include:

- Immediate
- Immediate extended
- Modified page zero
- Relative
- Extended
- Indexed
- Register
- Register indirect
- Implied

8-Bit Load Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments	
LD r,r'	r ← r'	.	.	X	.	X	.	.	.	01	r	r'		1	1	4	r,r'	Reg.
LD r,n	r ← n	.	.	X	.	X	.	.	.	00	r	110		2	2	7	000	B
										←	n	→					001	C
LD r,(HL)	r ← (HL)	.	.	X	.	X	.	.	.	01	r	110		1	2	7	010	D
LD r,(IX+d)	r ← (IX+d)	.	.	X	.	X	.	.	.	11	011	101	DD	3	5	19	011	E
										01	r	101					100	H
										←	d	→					101	L
LD r,(IY+d)	r ← (IY+d)	.	.	X	.	X	.	.	.	11	111	101	FD	3	5	19	111	A
										01	r	110						
										←	d	→						
LD (HL),r	(HL) ← r	.	.	X	.	X	.	.	.	01	110	r		1	2	7		
LD (IX+d),r	(IX+d) ← r	.	.	X	.	X	.	.	.	11	011	101	DD	3	5	19		
										01	110	r						
										←	d	→						
LD (IY+d),r	(IY+d) ← r	.	.	X	.	X	.	.	.	11	111	101	FD	3	5	19		
										01	110	r						
										←	d	→						
LD (HL), n	(HL) ← n	.	.	X	.	X	.	.	.	00	110	110	36	2	3	10		
										←	n	→						
LD (IX+d), n	(IX+d) ← n	.	.	X	.	X	.	.	.	11	011	101	DD	4	5	19		
										00	110	110	36					
										←	d	→						
										←	n	→						
LD (IY+d), n	(IY+d) ← n	.	.	X	.	X	.	.	.	11	111	101	FD	4	5	19		
										00	110	110	36					
										←	d	→						
										←	n	→						

LD A, (BC)	A ← (BC)	.	.	X	.	X	.	.	.	00	001	010	0A	1	2	7
LD A, (DE)	A ← (DE)	.	.	X	.	X	.	.	.	00	011	010	1A	1	2	7
LD A, (nn)	A ← (nn)	.	.	X	.	X	.	.	.	00	111	010	3A	3	4	13
										←	n	→				
										←	n	→				
LD (BC), A	(BC) ← A	.	.	X	.	X	.	.	.	00	000	010	02	1	2	7
LD (DE), A	(DE) ← A	.	.	X	.	X	.	.	.	00	010	010	12	1	2	7
LD (nn), A	(nn) ← A	.	.	X	.	X	.	.	.	00	110	010	32	3	4	13
										←	n	→				
										←	n	→				
LD A, I	A ← I	↕	↕	X	0	X	IFF	0	.	11	101	101	ED	2	2	9
										01	010	111	57			
LD A, R	A ← R	↕	↕	X	0	X	IFF	0	.	11	101	101	ED	2	2	9
										01	011	111	5F			
LD I, A	I ← A	.	.	X	.	X	.	.	.	11	101	101	ED	2	2	9
										00	000	111	47			
LD R, A	R ← A	.	.	X	.	X	.	.	.	11	101	101	ED	2	2	9
										01	001	111	4F			

NOTES: r,r' means any of the registers A, B, C, D, E, H, L.

IFF the content of the interrupt enable flip-flop, (IFF) is copied into the P/V flag.

For an explanation of flag notation and symbols for mnemonic tables, see Symbolic Notation section following tables.

16-Bit Load Group

Mnemonic	Symbolic Operations	S	Z	H	P/V	N	C	Opcode 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD dd, nn	dd ← nn	.	.	X	.	X	.	.	.	00	dd0	001		3	3	10	dd Pair 00 BC
								←	n	→					01 DE
								←	n	→					10 HL
LD IX, nn	IX ← nn	.	.	X	.	X	.	.	.	11	011	101	DD	4	4	14	11 SP
								00	100	001	21				
								←	n	→					
								←	n	→					
LD IY, nn	IY ← nn	.	.	X	.	X	.	.	.	11	111	101	FD	4	4	14	
								00	100	001	21				
								←	n	→					
								←	n	→					
LD HL, (nn)	H ← (nn+1) L ← (nn)	.	.	X	.	X	.	.	.	00	101	010	2A	3	5	16	
								←	n	→					
								←	n	→					
LD dd, (nn)	dd_H ← (nn+1) dd_L ← (nn)	.	.	X	.	X	.	.	.	11	101	101	ED	4	6	20	
								01	dd1	011					
								←	n	→					
								←	n	→					
LD IX, (nn)	IX_H ← (nn+1) IX_L ← (nn)	.	.	X	.	X	.	.	.	11	011	101	DD	4	6	20	
								00	101	010	2A				
								←	n	→					
								←	n	→					
LD (nn), HL	(nn+1) ← H (nn) ← L	.	.	X	.	X	.	.	.	00	100	010	22	3	5	16	
								←	n	→					
								←	n	→					
LD (nn), dd	(nn+1) ← dd_H (nn) ← dd_L	.	.	X	.	X	.	.	.	11	101	101	ED	4	6	20	
								01	dd0	011					
								←	n	→					
								←	n	→					

LD (nn), IX	(nn+1) ← IX_H	.	.	X	.	X	.	.	.	11	011	101	DD	4	6	20	
	(nn) ← IX_L									00	100	010	22				
										←	n	→					
										←	n	→					
LD SP, HL	SP ← HL	.	.	X	.	X	.	.	.	11	111	001	F9	1	1	6	
LD SP, IX	SP ← IX	.	.	X	.	X	.	.	.	11	011	101	DD	2	2	10	
										11	111	001	F9				
LD SP, IY	SP ← IY	.	.	X	.	X	.	.	.	11	111	101	FD	2	2	10	
										11	111	001	F9				
PUSH qq	(SP-2) ← qqL	.	.	X	.	X	.	.	.	11	qq0	101		1	3	11	
	(SP-1) ← qqH																
	SP - SP-2																
PUSH IX	(SP-2) - IX	.	.	X	.	X	.	.	.	11	011	101	DD	2	4	15	
	(SP-1) - IX									11	100	101	E5				
	SP → SP-2																
PUSH IY	(SP-2) ← IY_L	.	.	X	.	X	.	.	.	11	111	101	FD	2	4	15	
	(SP-1) ← IY_H									11	100	101	E5				
POP qq	qqH ← (SP+1)	.	.	X	.	X	.	.	.	11	qq0	001		1	3	10	
	qqL ← (SP)																
	SP → SP+2																
POP IX	IX_H ← (SP+1)	.	.	X	.	X	.	.	.	11	011	101	DD	2	4	14	
	IX_L ← (SP)									11	100	001	E1				
	SP → SP+2																
POP IY	IY_H ← (SP+1)	.	.	X	.	X	.	.	.	11	111	101	FD	2	4	14	
	IY_L ← (SP)									11	100	001	E1				
	SP → SP+2																

qq	Pair
00	BC
01	DE
10	HL
11	AF

NOTES: dd is any of the register pairs BC, DE, HL, SP.

qq is any of the register pairs AF, BC, DE, HL.

$(PAIR)_H$, $(PAIR)_L$ refer to high order and low order eight bits of the register pair respectively. e.g., BC_L = C, AF_H = A

Exchange, Block Transfer, Block Search Groups

Mnemonic	Symbolic Operation	S	Z		Flags H		P/V	N	C	Opcode 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
EX DE, HL	DE ↔ HL	.	.	X	.	X	.	.	.	11	101	011	EB	1	1	4	
EX AF, AF'	AF ↔ AF'	.	.	X	.	X	.	.	.	00	001	000	08	1	1	4	
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	.	.	X	.	X	.	.	.	11	011	001	D9	1	1	4	Register bank and auxiliary register bank exchange
EX (SP), HL	H ↔ (SP+1) L ↔ (SP)	.	.	X	.	X	.	.	.	11	100	011	E3	1	5	19	
EX (SP), IX	IX_H ↔ (SP+1) IX_L ↔ (SP)	.	.	X	.	X	.	.	.	11 11	011 100	101 011	DD E3	2	6	23	
EX (SP), IY	IY_H ↔ (SP) IY_L ↔ (SP)	.	.	X	.	X	.	.	.	11 11	111 100	101 011	FD E3	2	6	23	
LDI	(DE) ← (HL) DE ← DE+1 HL ← HL+1 BC ← BC−1	.	.	X	.	X	① ↕	0	.	11 10	101 100	101 000	ED A0	2	4	16	Load (HL) into (DE), increment the pointers and decrement the byte counter (BC)
LDIR	(DE) ← (HL) DE ← DE+1 HL ← HL+1 BC ← BC−1 Repeat until BC = 0	.	.	X	0	X	0	0	.	11 10	101 110	101 000	ED B0	2 2	5 4	21 16	If BC ≠ 0 If BC = 0

LDD	(DE) ← (HL) DE ← DE−1 HL ← HL−1 BC ← BC−1	.	.	X	0	X	①↕	0	.	11 10	101	101	ED A8	2	4	16	
LDDR	(DE) ← (HL) DE ← DE−1 HL ← HL−1 BC ← BC−1 Repeat until BC = 0	.	.	X	0	X	0	0	.	11 10	101	101	ED B8	2 2	5 4	21 16	If BC ≠ 0 If BC = 0
CPI	A ← (HL) HL ← HL+1 BC ← BC−1	↕	②↕	X	↕	X	①↕	1	.	11 10	101	101	ED A1	2	4	16	
CPIR	A − (HL) HL ← HL+1 BC ← BC−1 Repeat until A = (HL) or BC = 0	↕	②↕	X	↕	X	①↕	1	.	11 10	101	101	ED B1	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)
CPD	A − (HL) HL ← HL−1 BC ← BC−1	↕	②↕	X	↕	X	①↕	1	.	11 10	101	101	ED A9	2	4	16	

CPDR	A - (HL)	↕	②↕	X	↕	X	①↕	1	.	11	101	101	ED	2	5	21	If BC ≠ 0 and A ≠ (HL)
	HL ← HL-1 BC ← BC-1 Repeat until A = (HL) or BC = 0									10	111	001	B9	2	4	16	If BC = 0 or A = (HL)

NOTES: ① P/V flag is 0 if the result of BC-1 = 0, otherwise P/V = 1

② Z flag is 1 if A = (HL), otherwise Z = 0

8-Bit Arithmetic and Logical Group

Mnemonic	Symbolic Operation	S	Z		Flags H		P/V	N	C	Opcode 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments r	Reg.
ADD A, r	A ← A+r	↕	↕	X	↕	X	V	0	↕	10	000	r		1	1	4		
ADD A, n	A ← A+n	↕	↕	X	↕	X	V	0	↕	11	000	110		2	2	7	000	B
										←	n	→					001	C
																	010	D
ADD A, (HL)	A ← A+(HL)	↕	↕	X	↕	X	V	0	↕	10	000	110		1	2	7	011	E
ADD A1 (IX+d)	A ← A+(IX+d)	↕	↕	X	↕	X	V	0	↕	11	011	101	DD	3	5	19	100	H
										10	000	110					101	L
										←	d	→						
ADD A, (IY+d)	A ← A+(IY+d)	↕	↕	X	↕	X	V	0	1	11	111	101	FD	3	5	19		
										10	000	110						
										←	d	→						

ADC A, s	A ← A+s+CY	↕	↕	X	↕	X	V	0	↕		001					s is any of r, n, (HL), (IY+d) as shown for ADD instructions. The indicated bits replace the 000 in ADD set above.
SUB s	A ← A-s	↕	↕	X	↕	X	V	1	↕		010					
SBC A, s	A ← A-s-CY	↕	↕	X	↕	X	V	1	↕		011					
AND s	A ← A ∧ s	↕	↕	X	↕	X	P	0	0		100					
OR s	A ← A ∨ s	↕	↕	X	0	X	P	0	0		110					
XOR s	A ← A ⊕ s	↕	↕	X	0	X	P	0	0		101					
CP s	A - s	↕	↕	X	↕	X	V	1	↕		111					
INC r	r ← r+1	↕	↕	X	↕	X	V	0	.	00	r	100		1	1	4
INC (HL)	(HL) ← (HL+1)	↕	↕	X	↕	X	V	0	.	00	110	100		1	3	11
INC (IX+d)	(IX+d) ←	↕	↕	X	↕	X	V	0	.	11	011	101	DD	3	6	23
	(IX+d) + 1									00	110	100				
										←	d	→				
INC (IY+d)	(IY+d) ←	↕	↕	X	↕	X	V	0	.	11	111	101	FD	3	6	23
	(IY+d)+1									00	110	100				
										←	d	→				

DEC m	m ← m−1	↕	↕	X	↕	X	V	1	.	101	m is any of r, (HL), (IX+d), (IY+d) as shown for INC. DEC same format and states as INC. Replace 100 with 101 in opcode.

General-Purpose Arithmetic and CPU Control Groups

Mnemonic	Symbolic Operation	Flags S	Z		H		P/V	N	C	Opcode 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
DAA	Converts acc. content into packed BCD following add or subtract with packed BCD operands.	↕	↕	X	↕	X	P	.	↕	00	100	111	27	1	1	4	Decimal adjust accumulator
CPL	$A \leftarrow \overline{A}$	.	.	X	↕	X	.	1	.	00	101	111	2F	1	1	4	Complement accumulator (one's complement).
NEG	$A \leftarrow 0 - A$	↕	↕	X	↕	X	V	1	↕	11 01	101 000	101 100	ED 44	2	2	8	Negate acc. (two's complement).
CCF	$CY \leftarrow \overline{CY}$	.	.	X	X	X	.	0	↕	00	111	111	3F	1	1	4	Complement carry flag.
SCF	$CY \leftarrow 1$	.	.	X	0	X	.	0	1	00	110	111	37	1	1	4	Set carry flag.

NOP	No operation	.	.	X	.	X	.	.	.	00	000	000	00	1	1	4
HALT	CPU halted	.	.	X	.	X	.	.	.	01	110	110	76	1	1	4
D1*	IFF ← 0	.	.	X	.	X	.	.	.	11	110	011	F3	1	1	4
E1*	IFF ← 1	.	.	X	.	X	.	.	.	11	111	011	FB	1	1	4
IMO	Set interrupt	.	.	X	.	X	.	.	.	11	101	101	ED	2	2	8
	mode 0									01	000	110	46			
IM1	Set interrupt	.	.	X	.	X	.	.	.	11	101	101	ED	2	2	8
	mode 1															
IM2	Set interrupt	.	.	X	.	X	.	.	.	11	101	101	ED	2	2	8
	mode 2									01	011	110	5E			

NOTES: IFF indicates the interrupt enable flip flop.

CY indicates the carry flip flop.

* indicates interrupts are not sampled at the end of EI or DI.

16-Bit Arithmetic Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD HL, ss	HL ← HL+ss	.	.	X	X	X	.	0	↕	00	ss1	001		1	3	11	ss Reg. 00 BC
ADC HL, ss	HL ← HL+ss+CY	↕	↕	X	X	X	V	0	↕	11	101	101	ED	2	4	15	01 DE
										01	ss1	010					10 HL
																	11 SP
SBC HL, ss	HL ← HL−ss−CY	↕	↕	X	X	X	V	1	↕	11	101	101	ED	2	4	15	
										01	ss0	010					
ADD IX, pp	IX ← IX+pp	.	.	X	X	X	.	0	↕	11	011	101		2	4	15	pp Reg. 00 BC
										01	pp1	001					01 DE
																	10 IX
																	11 SP
ADD IY, rr	IY ← IY+rr	.	.	X	X	X	.	0	↕	11	111	101	FE	2	4	15	rr Reg. 00 BC
										00	rr1	001					01 DE
																	10 IY
																	11 SP
INC ss	ss ← ss+1	.	.	X	.	X	.	.	.	00	ss0	011		1	1	6	
INC IX	IX ← IX+1	.	.	X	.	X	.	.	.	11	011	101	DD	2	2	10	
										00	100	011	23				
INC IY	IY ← IY+1	.	.	X	.	X	.	.	.	11	111	101	FD	2	2	10	
										00	100	011	23				

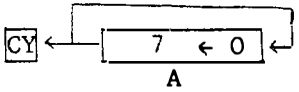
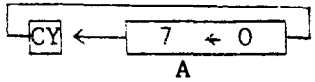
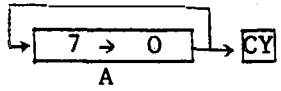
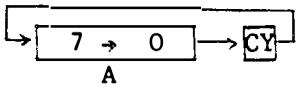
DEC ss	ss ← ss-1	.	.	X	.	X	.	.	.	00	ss1	011		1		1	6
DEC IX	IX ← IX-1	.	.	X	.	X	.	.	.	11	011	101	DD	2		2	10
										00	101	011	2B				
DEC IY	IY ← IY-1	.	.	X	.	X	.	.	.	11	111	101	FD	2		2	10
										00	101	011	2B				

NOTES: ss is any of the register pairs BC, DE, HL, SP.

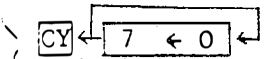
pp is any of the register pairs BC, DE, IX, SP.

rr is any of the register pairs BC, DE, IY, SP.

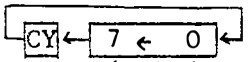
Rotate and Shift Group

Mnemonic	Symbolic Operation	S	Z		Flags H		P/V	N	C	76	Opcode 543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RLCA		.	.	X	0	X	.	0	↕	00	000	111	07	1	1	4	Rotate left circular accumulator.
RLA		.	.	X	0	X	.	0	↕	00	010	111	17	1	1	4	Rotate left accumulator.
RRCA		.	.	X	0	X	.	0	↕	00	001	111	OF	1	1	4	Rotate right circular accumulator.
RRA		.	.	X	0	X	.	0	↕	00	011	111	IF	1	1	4	Rotate right accumulator.

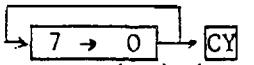
RLCr	↕	↕	X	0	X	P	0	↕	11 001 011 00 000 r	CB	2	2	8	Rotate left circular register r.
RLC (HL)	↕	↕	X	0	X	P	0	↕	11 001 011 00 000 110	CB	2	4	15	r Reg. 000 B 001 C 010 D
RLC (IX+d)	↕	↕	X	0	X	P	0	↕	11 011 101 11 001 011 ← d → 00 000 110	DD CB	4	6	23	011 E 100 H 101 L 111 A
RKC (IY+d)	↕	↕	X	0	X	P	0	↕	11 111 101 11 001 011 ← d → 00 000 110	FD CB	4	6	23	
RL m	↕	↕	X	0	X	P	0	↕	010					Instruction format and states are as shown for RLC's. To form new opcode replace 000 or RLC's with shown code.
RRC m	↕	↕	X	0	X	P	0	↕	001					



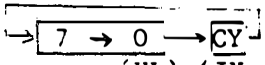
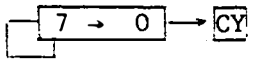
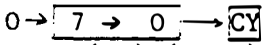
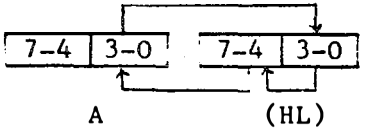
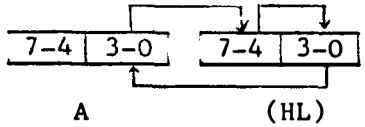
r,(HL),(IX+d),(IY+d)



m r,(HL),(IX+d),(IY+d)



m r,(HL),(IX+d),(IY+d)

RR m		↕	↕	X	0	X	P	0	↕				011			
	m r,(HL),(IX+d),(IY+d)															
SLA m		↕	↕	X	0	X	P	0	↕				100			
	m r,(HL),(IX+d),(IY+d)															
SRA m		↕	↕	X	0	X	P	0	↕				101			
	m r,(HL),(IX+d),(IY+d)															
SRL m		↕	↕	X	0	X	P	0	↕				111			
	m ≡ r,(HL),(IX+d),(IY+d)															
RLD		↕	↕	X	0	X	P	0	.	11 01	101 101	101 111	ED 6F	2	5	18	Rotate digit left and right between the accumulator and location (HL).
RRD		↕	↕	X	0	X	P	0	.	11 01	101 100	101 111	ED 67	2	5	18	The content of the upper half of the accumulator is unaffected.

Bit Set. Reset and Test Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	comments
BIT b,r	$Z \leftarrow \overline{r_b}$	X	↕	X	↕	X	X	0	.	11	001	011	CB	2	2	8	r Reg. 000 B
								01		b	r						
BIT b,(HL)	$Z \leftarrow (\overline{HL})_b$	X	↕	X	↕	X	X	0	.	11	001	011	CB	2	3	12	001 C 010 D
								01		b	110						
BIT b,(IX+d)	$Z \leftarrow (\overline{IY+d})_b$	X	↕	X	↕	X	X	0	.	11	011	101	DD	4	5	20	011 E 100 H 101 L 111 A
										11	001	011	CB				
										←	d	→					
								01		b	110						
BIT b,(IY+d)	$Z \leftarrow (\overline{IY+d})_b$	X	↕	X	↕	X	X	0	.	11	111	101	FD	4	5	20	b Bit Tested 000 0 001 1 010 2 011 3 100 4 101 5 110 6 111 7
										11	001	011	CB				
										←	d	→					
								01		b	110						
SET b,r	$r_b \leftarrow 1$	.	.	X	.	X	.	.	.	11	001	011	CB	2	2	8	
										11	b	r					
SET b,(HL)	$(HL)_b \leftarrow 1$	.	.	X	.	X	.	.	.	11	001	011	CB	2	4	15	
										11	b	110					

SET b,(IX+d)	$(IX+d)_b$	← 1	.	.	X	.	X	.	.	.	11 11 ←	011 001 d	101 011 →	DD CB	4		6		23		
											11	b	110								
RES b,m	m_b ← 0 m ≡ r,(HL), (IX+d), (IY+d)		.	.	X	.	X	.	.	.	10									To form new opcode replace 11 of SET b, s with 10. Flags and time states for SET instruction.	

NOTES: The notation m_b indicates bit b (0 to 7) or location m.

Jump Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
JP nn	PC ← nn	.	.	X	X	.	.	11	000	011	C3	3	3	10	
								←	n	→					
								←	n	→					cc Condition
JP cc, nn	If condition cc is true PC ← nn, otherwise continue	.	.	X	X	.	.	11	cc	010		3	3	10	000 NZ non-zero
								←	n	→					001 Z zero
								←	n	→					010 NC non-carry
															011 C carry
															100 PO parity odd
															101 PE parity even
															110 P sign positive
JR e	PC ← PC+e	.	.	X	X	.	.	00	011	000	18	2	3	12	111 M sign negative
								←	e-2	→					
JR C,e	If C = 0, continue	.	.	X	X	.	.	00	111	000	38	2	2	7	If condition not met.
								←	e-2	→					
	If C = 1, PC ← PC+e											2	3	12	If condition is met.

JR NC,e	If C = 1, continue	.	.	X	.	X	.	.	.	00 ←	110 e-2	000 →	30	2	2	7	If condition not met.
	If C = 0, PC ← PC+e													2	3	12	If condition is met.
JP Z,e	If Z = 0, continue	.	.	X	.	X	.	.	.	00 ←	101 e-2	000 →	28	2	2	7	If condition not met.
	If Z = 1, PC ← PC+e													2	3	12	If condition is met.
JR NZ,e	If Z = 1, continue	.	.	X	.	X	.	.	.	00 ←	100 e-2	000 →	20	2	2	7	If condition not met.
	If Z = 0, PC ← PC+e													2	3	12	If condition is met.
JP (HL)	PC ← HL	.	.	X	.	X	.	.	.	11	101	001	E9	1	1	4	
JP (IX)	PC ← IX	.	.	X	.	X	.	.	.	11	011	101	DD	2	2	8	
										11	101	001	E9				
JP (IY)	PC ← IY	.	.	X	.	X	.	.	.	11	111	101	FD	2	2	8	
										11	101	001	E9				
DINZ,e	B ← B-1	.	.	X	.	X	.	.	.	00 ←	010 e-2	000 →	10	2	2	8	If B = 0
	If B = 0, continue																
	If b ≠ 0, PC ← PC+e													2	3	13	If B = 0

NOTES: e represents the extension in the relative addressing mode.

e is a signed two's complement number in the range < -126, 129 >.

e - 2 in the opcode provides an effective address of pc+e as PC is incremented by 2 prior to the addition of e.

Call and Return Group

Mnemonic	Symbolic Operation	S	Z		H		P/V	N	C	76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
CALL nn	$(SP-1) \leftarrow PC_H$	.	.	X	.	X	.	.	.	11	001	101	CD	3	5	17	
	$(SP-2) \leftarrow PC_L$									←	n	→					
	PC ← nn									←	n	→					
CALL cc,nn	If condition cc is false continue,	.	.	X	.	X	.	.	.	11	cc	100		3	3	10	If cc is false.
										←	n	→					
	otherwise same as CALL nn									←	n	→		3	5	17	If cc is true.
RET	PC ← (SP)	.	.	X	.	X	.	.	.	11	001	001	C9	1	3	10	
	PC ← (SP+1)																
RET cc	If condition cc is false continue,	.	.	X	.	X	.	.	.	11	cc	000		1	1	5	If cc is false.
	otherwise same as RET													1	3	11	If cc is true.

RETI	Return from interrupt	.	.	X	.	X	.	.	.	11 01	101 001	101 101	ED 4D	2	4	14
RETN[1]	Return from non-maskable interrupt	.	.	X	.	X	.	.	.	11 01	101 000	101 101	ED 45	2	4	14
RST p	(SP-1) ← PC_H (SP-2) ← PC_L PC_H ← 0 PC_L ← p	.	.	X	.	X	.	.	.	11	t	111		1	3	11

cc	Condition
000	NZ non-zero
001	Z zero
010	NC non-carry
011	C carry
100	PO parity odd
101	PE parity even
110	P sign positive
111	M sign negative

t	p
000	00H
001	08H
010	10H
011	18H
100	20H
101	28H
110	30H
111	38H

NOTE: RETN loads IFF_2 - IFF_1

Input and Output Group

Mnemonic	Symbolic Operation	S	Z	X	H	X	P/V	N	C	Opcode 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
IN A,(n)	A ← (n)	.	.	X	.	X	.	.	.	11	011	011	DB	2	3	11	n to A_0 - A_7 Acc. to A_8 - A_{15}
										←	n	→					
IN r,(C)	r ← (C) if r = 110 only the flags will be affected	↕	↕	X	↕	X	P	0	.	11 01	101 r	101 000	ED	2	3	12	C to A_0 - A_7 B to A_8 - A_{15}
INI	(HL) ← (C) B ← B-1 HL ← HL+1	X	① ↕	X	X	X	X	↕	.	11 10	101 100	101 010	ED A2	2	4	16	C to A_0 - A_7 B to A_8 - A_{15}
INIR	(HL) ← (C) B ← B-1 HL ← HL+1 Repeat until B = 0	X	↕	X	X	X	X	↕	.	11 10 	101 101 	101 010 	ED B2 	2 2	5 (If B ≠ 0) 4 (If B = 0)	21 16	C to A_0 - A_7 B to A_8 - A_{15}
IND	(HL) ← (C) B ← B-1 HL ← HL-1	X	① ↕	X	X	X	X	↕	.	11 10	101 101	101 010	ED AA	2	4	16	C to A_0 - A_7 B to A_8 - A_{15}
INDR	(HL) ← (C) B ← B-1 HL ← HL-1 Repeat until B = 0	X	↕	X	X	X	X	↕	.	11 10 	101 111 	101 010 	ED BA 	2 2	5 (If B ≠ 0) 4 (If B = 0)	21 16	C to A_0 - A_7 B to A_8 - A_{15}

OUT (C),r	(C) ← r	.	.	X	.	X	.	.	.	11	101	101	ED	2		3	12	C to A_0 - A_7
										01	r	001						B to A_8 - A_{15}
			1															
OUT1	(C) ← (HL)	X	↕	X	X	X	X	↕	.	11	101	101	ED	2		4	16	C to A_0 - A_7
	B ← B-1									10	100	011	A3					B to A_8 - A_{15}
	HL ← HL+1																	
OTIR	(C) ← (HL)	X	↕	X	X	X	X	↕	.	11	101	101	ED	2		5	21	C to A_0 - A_7
	B ← B-1									10	110	011	B3		(If B ≠ 0)			B to A_8 - A_{15}
	HL ← HL+1													2		4	16	
	Repeat until														(If B = 0)			
	B = 0																	
			1															
OUTD	(C) ← (HL)	X	↕	X	X	X	X	↕	.	11	101	101	ED	2		4	16	C to A_0 - A_7
	B ← B-1									10	101	011	AB					B to A_8 - A_{15}
	HL ← HL-1																	
OTDR	(C) ← (HL)	X	↕	X	X	X	X	↕	.	11	101	101	ED	2		5	21	C to A_0 - A_7
	B ← B-1									10	111	011			(If B ≠ 0)			B to A_8 - A_{15}
	HL ← HL-1													2		4	16	
	Repeat until																	
	B = 0														(If B = 0)			

NOTE: ① If the result of B-1 is zero the Z flag is set, otherwise it is reset.

Summary of Flag Operation

Instruction	D S	Z		H		P/V	N	D C	Comments
ADD A, s; ADC A, s	↕	↕	X	↕	X	V	0	↕	8-bit add or add with carry.
SUB s; SBC A, s; CP s; NEG	↕	↕	X	↕	X	V	1	↕	8-bit subtract, subtract with carry, compare and negate accumulator.
AND s	↕	↕	X	↕	X	P	0	0	
OR s, XOR a	↕	↕	X	0	X	P	0	0	Logical operations.
INC s	↕	↕	X	↕	X	V	0	.	8-bit increment.
DEC s	↕	↕	X	↕	X	V	1	.	8-bit decrement.
ADD DD, ss	.	.	X	X	X	.	0	↕	16-bit add.
ADC HL, ss	↕	↕	X	X	X	V	0	↕	16-bit add with carry.
SBC HL, ss	↕	↕	X	X	X	V	1	↕	16-bit subtract with carry.
RKAM RKCAM RRA; RRCA	.	.	X	0	X	.	0	↕	Rotate accumulator.
RL m; RLC m; RR m; RRC m; SLA m; SRA m; SRL m	↕	↕	X	0	X	P	0	↕	Rotate and shift locations.
RLD; RRD	↕	↕	X	0	X	P	0	.	Rotate digit left and right.
DAA	↕	↕	X	↕	X	P	.	↕	Decimal adjust accumulator.
CPL	.	.	X	1	X	.	1	.	Complement accumulator.
SCF	.	.	X	0	X	.	0	1	Set carry.
CCF	.	.	X	X	X	.	0	↕	Complement carry.
IN r (C)	↕	↕	X	0	X	P	0	.	Input register indirect.
INI, IND, OUTI; OUTD	X	↕	X	X	X	X	↕	.	Block input and output, Z = 0 if B ≠ 0
INIR; INDR; OTIR; OTDR	X	1	X	X	X	X	1	.	otherwise Z = 0.
LDI; LDD	X	X	X	0	X	0	0	.	Block transfer instructions. P/V = 1 if BC ≠ 0,
LDIR; LDDR	X	X	X	0	X	0	0	.	otherwise P/V = 0.
CPI; CPIR; CPD; CPDR	X	↕	X	X	X	↕	1	.	Block search instructions, Z = 1 if A = (HL), otherwise Z = 0, P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LD A, I, LD A, R	↕	↕	X	0	X	IFF	0	.	The content of the interrupt enable flip-flop (IFF) is copied into P/V flag.
BIT b, s	X	↕	X	↕	X	X	0	.	The state of bit b of location is copied into the Z flag.

Symbolic Notation

Symbol	Operation
S	Sign flag. S = 1 if the MSB of the result is 1.
Z	Zero flag. Z = 1 if the result of the operation is 0.
P/V	Parity or overflow flag. Parity (P) and overflow (V) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If P/V holds parity, P/V = 1 if the result of the operation is even, P/V = 0 if result is odd. If P/V holds overflow, P/V = 1 if the result of the operation produced an overflow.
H	Half-carry flag. H = 1 if the add or subtract operation produced a carry into or borrow from bit 4 of the accumulator.
N	Add/Subtract flag. N = 1 if the previous operation was a subtract.
H & N	H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed BCD format following addition or subtraction using operands with packed BCD format.
C	Carry/Link flag. C = 1 if the operation produced a carry from the MSB of the operand or result.
↕	The flag is affected according to the result of the operation.
.	The flag is unchanged by the operation.
0	The flag is reset by the operation.
1	The flag is set by the operation.
X	The flag is a "don't care."
V	P/V flag affected according to the overflow result of the operation.
P	P/V flag affected according to the parity result of the operation.
r	Any one of the CPU registers A, B, C, D, E, H, L.
s	Any 8-bit location for all the addressing modes allowed for the particular instruction.

ss	Any 16-bit location for all the addressing modes allowed for that instruction.
ii	Any one of the two index registers IX or IY.
R	Refresh counter.
n	8-bit value in range <0,255>
nn	16-bit value in range <0,65535>

SVI-318 AND SVI-328 I/O PORT LOCATION

I/O PORT	R/W	DESCRIPTION	REMARK
10H	W	WRITE DATA PORT	PRINTER
11H	W	DATA STROBE	PRINTER
12H	R	STATUS (BIT 0 = "0" FOR READY)	PRINTER
20H	R	RECEIVER BUFFER REGISTER	MODEM
	W	DIVISOR LATCH (LEAST SIGNIFICANT)	MODEM
	W	TRANSMITTER HOLDING BUFFER REG.	MODEM
21H	W	DIVISOR LATCH (MOST SIGNIFICANT)	MODEM
	W	INTERRUPT ENABLE REGISTER	MODEM
22H	W	INTERRUPT IDENTIFICATION REGISTER	MODEM
23H	W	LINE CONTROL REGISTER	MODEM
24H	W	READ MODEM CONTROL REGISTER	MODEM
25H	R	LINE STATUS REGISTER	MODEM
26H	R	READ MODEM STATUS REGISTER	MODEM
28H	R	RECEIVER BUFFER REGISTER (LEAST SIGNIFICANT)	RS-232
	W	DIVISOR BUFFER REGISTER	RS-232
	W	TRANSMITTER HOLDING BUFFER REGISTER	RS-232
29H	W	DIVISOR LATCH (MOST SIGNIFICANT)	RS-232
	W	INTERRUPT ENABLE REGISTER	RS-232
2AH	W	INTERRUPT IDENTIFICATION REGISTER	RS-232
2BH	W	LINE CONTROL REGISTER	RS-232
2CH	W	MODEM CONTROL REGISTER	RS-232
2DH	R	LINE STATUS REGISTER	RS-232
30H	R	FD-1793 STATUS REGISTER	FLOPPY DISK
	W	FD-1793 COMMAND REGISTER	FLOPPY DISK
31H	R/W	FD-1793 TRACK REGISTER	FLOPPY DISK
32H	R/W	FD-1793 SECTOR REGISTER	FLOPPY DISK
33H	R/W	FD-1793 DATA REGISTER	FLOPPY DISK
34H	R	READ INTRQ AND DRQ O/P PINS	FLOPPY DISK
	W	DISK SELECT REGISTER (BIT 0 = "0" TO SELECT DISK 1 BIT 1 = "0" TO SELECT DISK 2)	FLOPPY DISK
38H	W	DENSITY SELECT REGISTER (BIT 0 = "0" FOR DOUBLE DEN. BIT 0 = "1" FOR SINGLE DEN.)	FLOPPY DISK
50H	W	ADDRESS REGISTER SELECT	80-COLUMN CARD
51H	W	CRT CONTROLLER REGISTER (R0-R17)	80-COLUMN CARD
58H	W	CRT BANK CONTROL (= OFFH BANK ON, = 00H BANK OFF)	80-COLUMN CARD
80H	W	TMS-9918A WRITE MODE=0	VDP
81H	W	TMS-9918A WRITE MODE=1	VDP
84H	R	TMS-9918A READ MODE=0	VDP
85H	R	TMS-9918A READ MODE=1	VDP
88H	W	AY-3-8910 LATCH ADDRESS	PSG
8CH	W	AY-3-8910 WRITE	PSG
90H	R	AY-3-8910 READ	PSG
96H	W	WRITE 8255 PORT C	PPI
97H	W	WRITE 8255 CONTROL WORD REGISTER	PPI
98H	R	READ 8255 PORT A	PPI
99H	R	READ 8255 PORT B	PPI

PIN DESCRIPTIONS

A_0- A_{15} - Address Bus (output, active High, 3-state). A_0- A_{15} form a 16-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 64K bytes) and for I/O device exchanges.

$\overline{BUSACK}$ - Bus Acknowledge (output, active Low). Bus Acknowledge indicates to the requesting device that the CPU address bus, data bus, and control signals $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ have entered their high-impedance states. The external circuitry can now control these lines.

$\overline{BUSREQ}$ - Bus Request (input, active Low). Bus Request has a higher priority than $\overline{NMI}$ and is alway recognized at the end of the current machine cycle. $\overline{BUSREQ}$ forces the CPU address bus, data bus, and control signals $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ to go to a high-impedance state so that other devices can control these lines. $\overline{BUSREQ}$ is normally wire-ORed and requires an external pullup for these applications. Extended $\overline{BUSREQ}$ periods due to extensive DMA operations can prevent the CPU from properly refreshing dynamic RAMs.

D_0- D_7 - Data Bus (input/output, active High, 3-state). D_0- D_7 constitute an 8-bit bidirectional data bus, used for data exchanges with memory and I/O.

$\overline{HALT}$ - Halt State (output, active Low). $\overline{HALT}$ indicates that the CPU has executed a Halt instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP to maintain memory refresh.

$\overline{INT}$ - Interrupt Request (input, active Low). Interrupt Request is generated by I/O devices. The CPU honors a request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled. $\overline{INT}$ is normally wire-ORed and requires an external pullup for these applications.

$\overline{IORQ}$ - Input/Output Request (output, active Low, 3-state). $\overline{IORQ}$ indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. $\overline{IORQ}$ is also generated concurrently with $\overline{M1}$ duridng an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.

$\overline{M1}$ - Machine Cycle One (output, active Low). $\overline{M1}$, together with $\overline{MREQ}$, indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. $\overline{M1}$, together with $\overline{IORQ}$, indicates an interrupt acknowledge cycle.

$\overline{MREQ}$ - Memory Request (output, active Low, 3-state). $\overline{MREQ}$ indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{NMI}$ - Non-Maskable Interrupt (input, active Low). $\overline{NMI}$ has a higher priority than $\overline{INT}$. $\overline{NMI}$ is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop, and automatically forces the CPU to restart at location 0066H.

$\overline{RD}$ - Memory Read (output, active Low, 3-state). $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{RESET}$ - Reset (input, active Low). $\overline{RESET}$ initializes the CPU as follows:

It resets the interrupt enable flip-flop, clears the PC and Registers I and R, and sets the interrupt status to Mode 0. During reset time, the address and data bus go to a high-impendance state, and all control output signals go to the inactive state. Note that $\overline{RESET}$ must be active for a minimum of three full clock cycles before the reset operation is completed.

$\overline{RFSH}$ - Refresh (output, active Low). $\overline{RFSH}$, together with $\overline{MREQ}$, indicates that the lower seven bits of the system's address bus can be used as a refresh address to the system's dynamic memories.

$\overline{WAIT}$ - Wait (input, active Low). $\overline{WAIT}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a Wait state as long as this signal is active. Extended $\overline{WAIT}$ periods can prevent the CPU from refreshing dynamic memory properly.

$\overline{WR}$ - Memory Write (output, active Low, 3-state). $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.

THE VIDEO DISPLAY PROCESSOR TMS-9918A OR 9929

TMS-9918A or 9929 VDP generates all control, synchronization and composite video signals. It also controls the storages, retrieval and refresh of the display data stored in the screen memory.

The VDP uses a 10.738 MHz crystal. It generates all required internal clock signal. The CPU Clock is supplied by the VDP and is obtained by dividing the 10.738 MHz Clock by 3.

There are three control signals, $\overline{CSW}$, $\overline{CSR}$ and 'MODE', from the MPU. These inputs are used to control the operating mode of the VDP. $\overline{CSW}$ is the MPU - to VDP write select signal. $\overline{CSR}$ is the MPU - to - VDP read select signal. 'MODE' is the signal which determines the source or destination of a read or write data transferred to the display memory RAM.

Video Display Modes

The VDP displays an image on the screen that can best be envisioned as a set of display planes sandwiched together. Figure 4-4 shows the definition of each of the planes. Objects on planes closest to the viewer have higher priority. In case where two entities on two different planes are occupying the same spot on the screen, the entity on the higher priority plane will show at that point. For an entity on a specific plane to show through, all planes in front of that plane must be transparent at that point. The first 32 planes (Figure 4-5) each may contain a single sprite. (Sprite are pattern objects whose positions on the screen are defined by horizontal and vertical coordinates in VRAM.) The areas of the Sprite Planes, outside of the sprite itself, are transparent. Since the coordinates of the sprite are in terms of pixels, the sprite can be positioned and moved about very accurately. Sprites are available in three sizes: 8 x 8 pixels, 16 x 16 pixels, and 32 x 32 pixels. Behind the Sprite Plane is the Pattern Plane. The Pattern Plane is used for textual and graphics images generated by the Text, Graphics I, Graphics II, or Multicolour modes. Behind the Pattern Plane is the backdrop, which is larger in area than the other planes so that it forms a border around the other planes. The last and lowest priority plane is the External Video Plane. Its image is defined by the external video input pin. The backdrop consists of a single colour used for the display borders and as the default colour for the active display area. The default colour is stored in the VDP register 7. When the backdrop colour register contains the transparent code, the backdrop automatically defaults to black if the external video mode is not selected.

The 32 Sprite Planes are used for the 32 sprites in the Multicolour and Graphics modes. They are not used in the Text mode and are automatically transparent. Each of the sprites can cover an 8 x 8, 16 x 16, or 32 x 32 pixel area on its plane. Any part of the plane not covered by the sprite is transparent. All or part of each sprite may also be transparent. Sprite 0 is on the outside or highest plane, and sprite 31 is on the plane immediately adjacent to Pattern Plane. Whenever a pixel in a Sprite Plane is transparent, the colour of the next plane can be seen through that plane. If, however, the sprite pixel is non-transparent, the colours of the lower planes are automatically replaced by the sprite colour. There is also a restriction on the number of sprites on a line. Only four sprites can be active on any horizontal line. Additional sprites on a line will be automatically made transparent for that line. Only those sprites that are active on the display will cause the coincidence flag to set. The VDP status register provides a flag bit and the number of the fifth sprite whenever this occurs. The Pattern Plane is used in the Text, Multicolour, and Graphics modes for display of the graphic patterns of characters. Whenever a pixel on the Pattern Plane is non-transparent, the backdrop colour is automatically replaced by the Pattern Plane colour. When a pixel in the Pattern Plane is transparent, the backdrop colour can be seen through the Pattern plane.

The VDP has four vided colour display modes that appear on the Pattern Plane: Graphics I mode, Graphics II mode, Text mode, and Multicolour mode. Graphics I and Graphics II modes cause the Pattern Plane to be broken up into groups of 8 x 8 pixels, called pattern positions. Since the full image is 256 x 192 pixels, there are 32 x 34 pattern positions on the screen in the graphic modes. In Graphics I mode, 256 possible patterns may be defined for the 768 pattern positions with two unique colours allowed for each pattern definition. Graphics II mode provides, through a unique mapping scheme, 768 pattern definations for the 768 pattern positions. Graphics II mode also allows the selection of two unique colours for each line of a pattern definition. Thus, all 15 colours plus transparent may be used in a single pattern position. In Text mode, the Pattern Plane is broken into groups of 6 x 8 pixels, called text positions. There are 40 x 24 text positions on the screen in this mode. In Text mode, sprites do not appear on the screen and two colours are defined for the entire screen. In Multicolour mode, the screen is broken into a grid of 64 x 48 positions, each of which is a 4 x 4 pixel. Within each position, one unique colour is allowed.

The VDP registers define the base addresses for several sub-blocks within VRAM. These sub-blocks form tables which are used to produce the desired image on the TV screen. The Pattern Name Table, the Pattern Generator Table and the Sprite Generator Table are used to form the sprites. The contents of these tables must all be provided by the microprocessor. Animation is achieved by altering the contents of VRAM in real time.

Signature	Description
CD0-CD7	CPU data bus (CD0) is the most significant bit
MODE	CPU interface mode select; usually a processor address line. Mode determines the source or destination of a read or write data transfer. Mode is normally tied to a CPU low order address read.
$\overline{CSR}$	CPU-VDP read strobe. $\overline{CSR}$ is the CPU-from-VDP read select. When it is active (low) the VDP outputs 8 bits on D0-D7 to the CPU.
$\overline{CSW}$	CPU-VDP write strobe. $\overline{CSW}$ is the CPU-from-VDP write select. When it is active (low), the 8 bits on D0-D7 are strobed into the VDP.
V_{cc}	+5 volt supply
V_{ss}	Ground Reference
RD0 RD7	VRAM read data bus (RD0 is the most significant bit)
AD0-AD7	VRAM address/data bus (multiplexed high and low order VRAM address and output data bytes) AD0 is the most significant bit and is used only for data and not for addressing.*
$\overline{RAS}$	VRAM row address strobe
$\overline{CAS}$	VRAM column address strobe
R/$\overline{W}$	VRAM write strobe
XTAL1, XTAL2	10.7 + MHz crystal inputs.**
GROMCLK	VDP output clock = XTAL/24. Typically not used
RESET/SYNC	$\overline{RESET}$ - This pin is a trilevel input pin. When it is below 0.8 volts, $\overline{RESET}$ initializes the VDP. When it is above 9 volts, $\overline{RESET}$ is the synchronizing input for external video. The VDP is externally initialized whenever the $\overline{RESET}$ input is active (low) and must be held low for a minimum of 3 microseconds. The external $\overline{RESET}$ synchronizes all clocks with its falling edge, sets the horizontal and vertical counters as known states, and clears VDP register 0 and 1. The video display is automatically blanked since the BLANK bit in VDP register 1 becomes a '0'. The VDP, however, continuous to refresh the VRAM even through the display is blanked. While the $\overline{RESET}$ is active, the VDP does not refresh VRAM.

Signature	Description
EXTVID	External video input
CPUCLK	NTSC colour burst frequency clock. Typically not used.
$\overline{INT}$	CPU interrupt output. The VDP $\overline{INT}$ output pin is used to generate an interrupt at the end of each active-display scan, which is about every 1/60 second (colour burst frequency/60, 192). The $\overline{INT}$ output is active when the interrupt enable bit (IE) in VDP register 1 is a '1' and the F bit of the status register is '1'. Interrupts are cleared when the status register is read.
COMVID	NTSC composite video output. The composite video output signal from the VDP drives on NTSC colour monitor. This signal incorporates all necessary horizontal and vertical synchronizations signals as well as luminance and chrominance information. In monitor applications, the requirements of the monitor should be studied to determine if the VDP can be connected directly to it. In some case, it may be necessary to provide a simple interface circuit to match the VDP output voltages with the monitor specifications. To drive a standard TV that is not outfitted with a composite video input, the signal can be run into the TV antenna terminals by using an appropriate RF modulator on the VDP output.

* The least-significant address bit, AD7, is wired to A0 of the dynamic RAMs. Likewise, AD6 is wired to A1 of the RAMs. Care must be exercised in assuring proper orientation of the TMS-9918A address outputs to the dynamic RAM address inputs.

** When driven externally, both inputs must be driven.

TMS-9929 Video Display Processor

This Preliminary Specification of the TMS-9929 is to be considered as an "ADD ON" to the basic TMS-9918 specification. The TMS-9929 is effectively identical to the TMS-9918 functionally and only has the colour video section that is different.

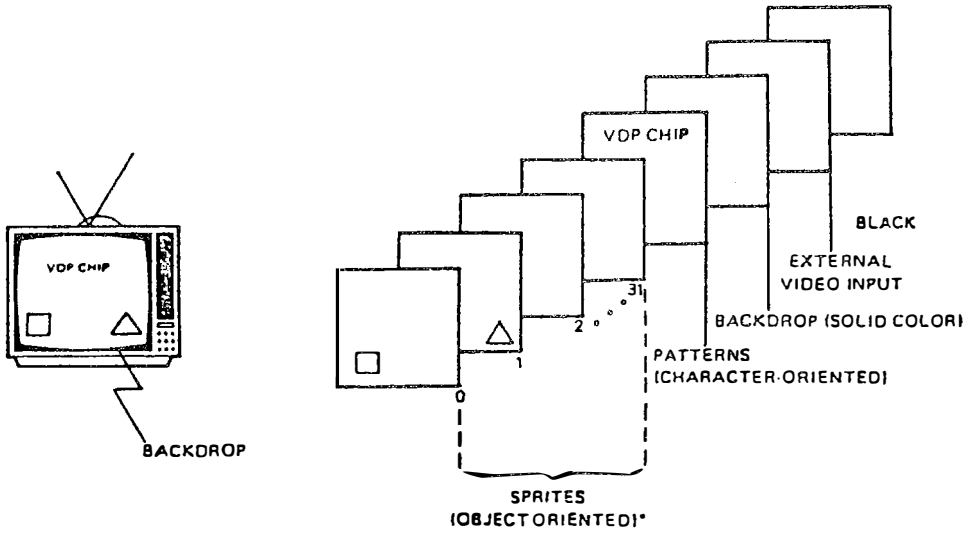
The TMS-9918 provides a composite colour video signal output that if driven by a suitable amplifier can go directly into any colour video monitor. The colour burst frequency is the VDP oscillator input frequency divided by three. External video mixing with an external reference source can also be achieved by inputting this external source directly into the TMS-9918.

In the TMS-9929 the colour and luminance/sync information is provided on three pins rather than a single pin in the form of two colour difference signals and, one luminance signal with all the vertical and horizontal timing included. So we have R-Y, B-Y, and Y respectively. The two colour difference signals are used then by an external quadrature modulator video encoder. It is outside the Video Display Processor that the composite colour video signal is generated into a PAL or Secam compatible TV signal. The external video mixing is also done outside and it is the TMS-9929 to decide when this mode is entered. This is achieved by a special level distinction made by the R-Y and B-Y VDP outputs. When external video is entered these two outputs go to the equivalent of the sync percentage level of the black-white swing in the luminance output, i.e. the colour difference outputs are normally swinging between the luminance blacm-white voltage levels and it is only in the external video mode that these outputs go to the reserved "sync" level.

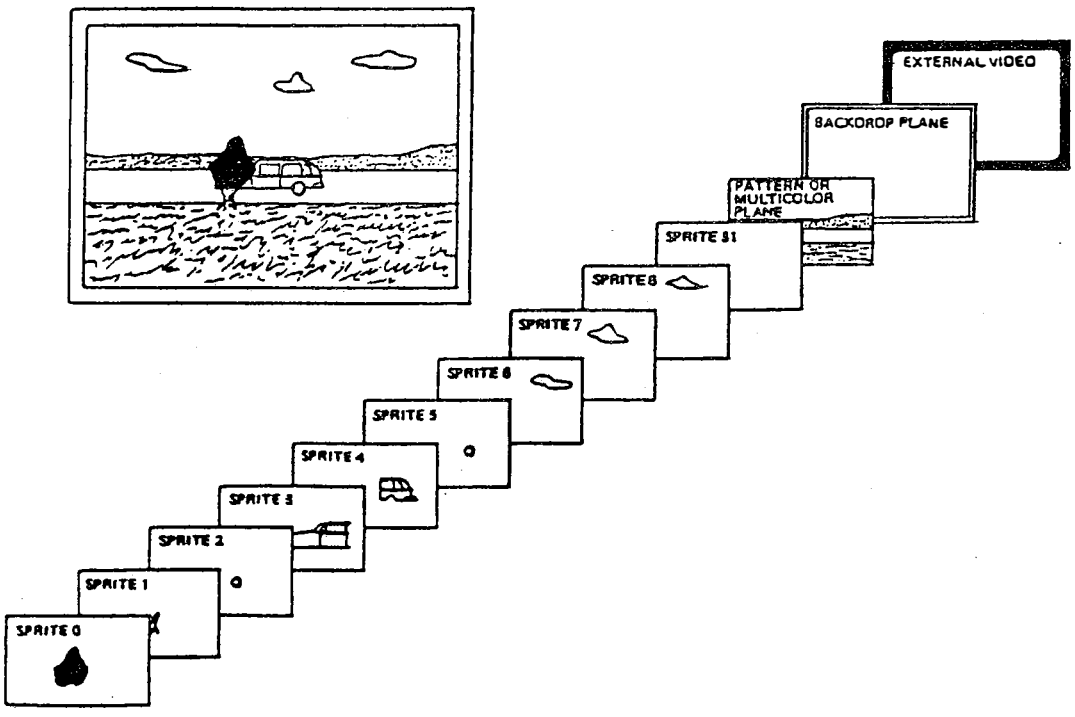
Phase locking of the VDP to the external PAL burst frequency is desirable if inter-hum or crawl effects want to be minimized. The TMS-9929 oscillator clock must still, however, be maintained within its prescribed limits of oscillator operation. CPUCLK signal is no longer available in the European TMS-9929.

The Programmable Sound Generator (PSG) is easily interfaced to any bus oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signalling and FSK modems. The analog sound outputs can each provide 4 bits of logarithmic digital to analog sound conversion, greatly enhancing the dynamic range of the sounds produced.

In order to perform sound effects while allowing the processor to continue its other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one effect is satisfied by the three independently controllable channels available in the PSG.



VDP DISPLAY PLANES
FIG. 4-4



VDP DISPLAY PLANES
FIG. 4-5

SVI-318/SVI-328 AND MARK II RAM/ROM DESCRIPTION

The SVI-318/SVI-328 and Mark II basic unit has 32K (80K)* bytes of Random Access Memory (RAM) divided into two group. Your instructions or programme to command the computer is stored in 16K (64K)* of RAM. Another 16K is strictly for use by the VDP to store display information (called VRAM).

The memory is comprised of eight 4116 (4164)* dynamic memory chips. The chips are refreshed every M1 cycle. RAM chip enable by the RAM block selectors. They go high to enable a block of RAM (8 RAM's per block) or during a REFCLK cycle to refresh the RAM's. Each RAM chip enable signal goes to the chip enable input for the respective block of RAM's.

RAM write from the R/W - O and MPX signal. When low the RAM's will accept data from the bus - the RAM's are reading the bus (R/W = O is high, read). When high the RAM's will output data to the bus - the RAM's are writing to the bus (R/W - O is low, write).

ROM

This memory is comprised of two 16K x 8 masked ROM chips. It contains the BASIC interpreter programme as well as the monitor programme.

For the SVI-318/SVI-328 and Mark II FCC sample and early production samples, these two ROM chips will be replaced by four 8K x 8 EPROMS chips and an additional small PCB carrying these four chips will be used to plug into the original ROM socket.

ROM bank control by the Bank Switch Address Decoder in the backpack. It enables the 32K ROM Bank on the CPU board, ROM 1 through ROM 8. With no backpack on ROM 1 through ROM 8 are always enabled.

* SVI-328

16384 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY (4116)

The 4116 is a 16384 words by 1 bit Dynamic MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

the 4116 is fabricated using a double-poly-layer N-channel silicon gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

Multiplexed address inputs permit the 4116 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

65536 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY (4864)

The 4864 utilizes a three-poly N-channel silicon gate process which provides high storage cell density, high performance and high reliability.

The 4864 uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, including the 512 sense amplifiers, which assures that power dissipation is minimized. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between Dynamic RAM generations.

The 4864 three-state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impendance state by returning $\overline{CAS}$ to a high state. The 4864 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to executed $\overline{RAS}$ only refresh cycles.

Refreshing is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of A_0 through A_6 during a 2 ms period.

Multiplexed address inputs permit the 4864 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

PROGRAMMABLE SOUND GENERATOR AY-3-8910

The AY-3-8910 is a register oriented programmable sound generator (PSG). Communication between the processor and the PSG is based on the concept of memory-mapped I/O. Control commands are issued to the PSG by writing to 16 memory-mapped registers. Each of the 16 registers within the PSG is also readable so that the microprocessor can determine, as necessary, present states or stored data values.

All functions of the PSG are controlled through its 16 registers which once programmed, generate and sustain the sounds, thus freeing the system processor for other tasks.

SOUND GENERATING BLOCK

The Basic Blocks in the PSG which produce the programmed sounds include:

Tone Generators	:	produce the basic square wave tone frequencies for each channel (A, B, C).
Noise Generator	:	produce a frequency modulated pseudo random pulse width square wave output.
Mixers	:	combine the outputs of the Tone Generators and the Noise Generator. One for each channel (A, B, C).
Amplitude Control	:	provides the D/A connectors with either a fixed or variable amplitude pattern. The fixed amplitude is under direct CPU control; the variable amplitude is accomplished by using the output of the Envelope Generator.
Envelope Generator	:	produces an envelope pattern which can be used to amplitude modulate the output of each mixer.
D/A Converters	:	the three D/A Converters each produce up to a 16 level output signal as determined by the Amplitude Control.

To output data from the CPU bus to a peripheral device connected to I/O Port A would require only the following steps:

1. Latch address R7 (select $\overline{\text{Enable}}$ register)
2. Write data to PSG (setting B6 of R7 to "1")
3. Latch address R16 (select 20A register)
4. Write data to PSG (data to be output on I/O Port A)

To input data from I/O Port A to the CPU bus would require the following:

1. Latch address R7 (select $\overline{\text{Enable}}$ register)

2. Write data to PSG (select B6 to R7 to "0")

3. Latch address R16 (select IOA register)

4. Read data from PSG (data from I/O Port A)

Note that once loaded with data in the input mode, the data will remain on the I/O Ports until changed either by loading different data, by applying a reset (grounding the Reset pin), or by switching to the input mode.

AY-3-8910 PROGRAMMABLE SOUND GENERATOR PIN ASSIGNMENTS

DA--DA0 (input/output/high impendance): pins 30--37

These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG and to receive data from the PSG. In the data mode, DA7--DA0 correspond to Register Array bits B7--B0. In the address mode, DA3--DA0 select the register #(0--17) and DA7--DA4 in conjunction with address inputs $\overline{\text{A9}}$ and A8 form the high order address (chip select).

A8 (input) : pin 25

$\overline{\text{A9}}$ (input) : pin 24

$\overline{\text{Address 9}}$, Address 8

These "extra" address bits are made available to enable the positioning of the PSG (assigning a 16 word memory space) in a total 1,024 word memory area rather than in a 256 word memory area as defined by address bits DA7--DA0 alone. If the memory size does not require the use of these extra address lines they may be left unconnected as each is provided with either an on-chip pull down (A9) or pull-up (A8) resistor. In "noisy" environments, however, it is recommended that $\overline{\text{A9}}$ and A8 be tied to an external ground and +5V, respectively, if they are not to be used.

$\overline{\text{RESET}}$ (input) : pin 23

For initialization/power-on purpose, applying a logic "0" (ground) to the Reset pin will reset all registers to "0". The $\overline{\text{Reset}}$ pin is provided with an on-chip pull-up resistor.

CLOCK (input) : pin 22

This TTL-compatible input supplies the timing reference for the Tone, Noise and Envelope Generators.

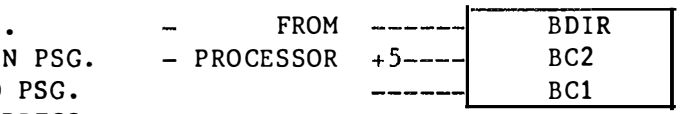
BDIR, BC2, BC1 (inputs) : pins 27, 28, 29

Bus DIRection, Bus Control 2, 1

These bus control signals are generated directly by Z80A series of microprocessors to control all external and internal bus operations in the PSG. When using a processor other than the Z80A, these signals can be provided either by comparable bus signals or by simulating the signals on I/O lines of the porcessor.

This could simplify the programming of the bus control signals to the following, which would only require that the processor generate two bus control signals (BDIR and BC1, with BC2 tied to +5V):

BDIR	BC2	BC1	PSG FUNCTION
0	1	0	INACTIVE.
0	1	1	READ FRIN PSG.
1	1	0	WRITE TO PSG.
1	1	1	LATCH ADDRESS



ANALOG CHANNEL A, B, C (output)

Each of these signals is the output of its corresponding mix of T4, and provides an up to 1V peak-peak signal representing the complex sound waveshape generated by the PSG.

IOA7--IOAO (input/output) : pins 14--21
IOB7--IOBO (input/output) : pins 6--13

Input/Output A7--AO, B7--BO

Each of these two parallel input/output ports provides 8 bits of parallel data to/from the PSG/CPU bus from/to any external devices connected to the IOA or IOB pins. Each pin is provided with an on-chip pull-up resistor, so that when in the "input" mode, all pins will read normally high. Therefore, the recommended method for scanning external switches, for example, would be to ground the input bit.

TEST 1 : pin 39

TEST 2 : pin 26

These pins are for user test purposes only and should be left open - do not use as tie-points.

V_{cc} : pin 40

Nominal +5 Volt power supply to the PSG.

V_{ss} : pin 1

Ground reference for the PSG.

The Programmable Sound Generator

The PSG AY-3-8190 generates all required sound under software control. There are two 8-bit I/O ports which are programmed as follow:

Port A : Programmed as input port and is used for the input signal from two joysticks controllers.

Port B : Programmed as output port which is used to output the bank control signals for the memory chips.

Detail signals for the ports are listed in the table below:

AY-3-8190 I/O Port A (Input Port)

		1 = No Contact
D0 ----	Joystick 1	0 = Forward
D1 ----	- do -	0 = Backward
D2 ----	- do -	0 = Left
D3 ----	- do -	0 = Right
D4 ----	Joystick 2	0 = Forward
D5 ----	- do -	0 = Backward
D6 ----	- do -	0 = Left
D7 ----	- do -	0 = Right

AY-3-8910 I/O Port B (Output Port)

D0 ---- Bank 1 (Game Cartridge)	0 = BANK ON
D1 ---- Bank 21	1 = BANK OFF
D2 ---- Bank 22	
D3 ---- Bank 31	
D4 ---- Bank 32	
D5 ---- Cap Lamp (Keyboard Cap Lock)	
D6 ---- ROM 2 enable (1 = Disable; 0 = Enable)	
D7 ---- ROM 3 enable (1 = Disable; 0 = Enable)	

THE PROGRAMMABLE PERIPHERAL INTERFACE 8255A

The 8255A PPI is used to strobe the keyboard lines, to interface the joystick fire button switch, the paddle and to control the cassette tape system. The ports are programmed as follow:

Port A : Programmed as input port. Bit 0-3 are used for the paddle input, bits 4 and 5 are used for the joystick fire switch input and bits 6 and 7 are used for signals from the cassette.

Port B : Programmed as output port and is used for keyboard read data.

Port C : Programmed as output port. Bits 0-3 outputs BCD data for keyboard scanning. Bits 4-6 outputs control signals for the cassette. Bit 7 is used to mix PSG sound data.

The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communication between the 8255A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

8255A BASIC OPERATION

A_0	A_1	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A ===⇒ DATA BUS
0	1	0	1	0	PORT B ===⇒ DATA BUS
1	0	0	1	0	PORT C ===⇒ DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS ===⇒ PORT A
0	1	1	0	0	DATA BUS ===⇒ PORT B
1	0	1	0	0	DATA BUS ===⇒ PORT C
1	1	1	0	0	DATA BUS ===⇒ CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS ===⇒ 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS ===⇒ 3-STATE

(RESET)

Reset. A "high" on this input clears the control register and all ports (A, C, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7-C4)
Control Group B - Port B and Port C lower (C3-C0)

The Control Word Register can only be written into. No Read operation of the Control Word Register is allowed.

Port A, B and C

The 8255A contains three 8-bit ports (A, B and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit port under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 - Basic Input/Output
Mode 1 - Strobed Input/Output
Mode 2 - Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impendance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system programme any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance, Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) - INTE is SET - Interrupt enable
(BIT-RESET) - INTE is RESET - Interrupt disable

Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

8255 Port A (Input Port)

```
D0  ----- Paddle or Tablet Input
D1  ----- Paddle or Tablet Input
D2  ----- Paddle or Tablet Input
D3  ----- Paddle or Tablet Input
D4  ----- Trigger Switch (Button) of Joystick 1 ] 0 = Pressed
D5  ----- Trigger Switch (Button) of Joystick 2 ] 1 = No Connect
D6  ----- Cassette Ready ( 0 = Ready, 1 = not ready )
D7  ----- Cassette Read Data
```

8255 Port B (Input Port)

```
D0 - D7  ----- Keyboard Read Data
```

8255 Port C (Output Port)

```
D0 - D3 -----  Keyboard BCD Output Data (For Keyboard Scanning)
D4      -----  Cassette Motor On (0 = Motor On, 1 = Motor Off)
D5      -----  Cassette Write Data
D6      -----  Cassette Audio Control (1 = Enable other channel in;
                                        (0 = Disable other channel in)
D7      -----  Mix PSG Sound Data
```

8255 Control Word (Write Only)

Initial Set	D7	D6	D5	D4	D3	D2	D1	D0
	1	0	0	1	0	0	1	0

INS8250-B FUNCTIONAL PIN DESCRIPTION

The following describes the function of all INS8250 input/output pins. Some of these descriptions reference internal circuits.

NOTE: In the following descriptions, a low represents a logic 0 (0 volt nominal) and a high represents a logic 1 (+2.4 volts nominal).

Input Signals

Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12-14: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{ADS}$) input. This enables communication between the INS8250 and the CPU.

Data Input Strobe (DISTR, $\overline{DISTR}$), Pins 22 and 21: When DISTR is high or $\overline{DISTR}$ is low while the chip is selected, allows the CPU to read status information or data from a selected register of the INS8250.

Note: Only an active DISTR or $\overline{DISTR}$ input is required to transfer data from the INS8250 during a read operation. Therefore, tie either the DISTR input permanently low or the $\overline{DISTR}$ input permanently high, if not used.

Data Output Strobe (DOSTR, $\overline{DOSTR}$), Pins 19 and 18: When DOSTR is high or $\overline{DOSTR}$ is low while the chip is selected, allows the CPU to write data or control words into a selected register of the INS8250.

Note: Only an active DOSTR or $\overline{DOSTR}$ input is required to transfer data to the INS8250 durisng a write operation. Therefore, tie either the DOSTR input permanently low or the $\overline{DOSTR}$ input permanently high, if not used.

Address Strobe ($\overline{ADS}$), Pin 25: When low, provides latching for the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals.

Note: An active $\overline{ADS}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.

Register Select (A0, A1, A2), Pins 26-28: These three inputs are used during a read or write operation to select an INS8250 register to read from or write into as indicated in the table below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain INS8250 registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

DLAB	A	A	A	REGISTER
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
x	0	1	0	Interrupt Identification (read only)
x	0	1	1	Line Control
x	1	0	0	MODEM Control
x	1	0	1	Line Status
x	1	1	0	MODEM Status
x	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significatnt byte)

Master Reset (MR), Pin 35: When high, clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the INS8250. Also, the state of various output signals (SOUT, INTRPT, OUT 1, OUT 2, RTS, DTR) are affected by an active MR input. (Refer to table 1).

Receiver Clock (RCLK), Pin 9: This input is the 16x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send ($\overline{\text{CTS}}$), Pin 36: The $\overline{\text{CTS}}$ signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{\text{CTS}}$ input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Set Ready ($\overline{DSR}$), Pin 37: When low, indicates that the MODEM or data set is ready to establish the communications link and transfer data with the INS8250. The $\overline{DSR}$ signal is MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Received Line Signal Detect ($\overline{RLSD}$), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{RLSD}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 7 (RLSD) of the MODEM Status Register. Bit 3 (DRLSD) of the MODEM Status Register indicates whether the $\overline{RLSD}$ input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the RLSD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Ring-Indicator ($\overline{RI}$), Pin 39: When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input has changed from a low to a high state since the previous reading of the MODEM Status Register.

Note: Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.

V_{cc} , Pin 40: +5-volt supply.

V_{ss} , Pin 20: Ground (0-volt) reference.

Output Signals

Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, informs the MODEM or data set that the INS8250 is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The $\overline{DTR}$ signal is set high upon a Master Reset operation.

Request to Send ($\overline{RTS}$), Pin 32: When low, informs the MODEM or data set that the INS8250 is ready to transmit data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The $\overline{RTS}$ signal is set high upon a Master Reset Operation.

Output 1 ($\overline{OUT\ 1}$), Pin 34: User-designed output that can be set to an active low by programming bit 2 ($\overline{OUT\ 1}$) of the MODEM Control Register to a high level. The $\overline{Out\ 1}$ signal is set high upon a Master Reset operation.

Chip Select Out (CSOUT), Pin 24: When high, indicates that the chip has been selected by active CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1.

Drive Disable (DDIS), Pin 23: Goes low whenever the CPU is reading data from the INS8250. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and INS8250 on the $D_7 - D_0$ Data Bus) at all times, except when the CPU is reading data.

Baud Out ($\overline{BAUDOUT}$), Pin 15: 16x clock signal for the transmitter section of the INS8250. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by typing this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag: Receiver Data Available: Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

INS8250 Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the li characteristics. The contents of the Line Control Register are indicated in table 2 and are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: this bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1-1/2 Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed).

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 a logic 0.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there regardless of other transmitter activity. The set break is disabled by setting bit 6 to a logic 0. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

INS8250 Programmable Baud Rate Generator

The INS8250 contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to $(2^{16} - 1)$. The output frequency of the Baud Generator is 16x the Baud rate [divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This previouss long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Rate Genertor with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

Note: The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56K Baud.

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the receer Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit No.	Register Address									
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter ter Holding Register (Write Only)	Interrupt Enable Register	Inter-Identi-fication Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	DLL	DLM
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmit-ter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indi-cator (TERI)	Bit 2	Bit 10

3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (PE)	Data Receiver Line Signal Detect (DRLSD)	Bit 2	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (TSRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 8	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSO)	Bit 7	Bit 15

Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference between Desired & Actual
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

Table 3. Baud Rates Using 1.8432 MHz Crystal.

Note: 1.8432 MHz is the standard 8080 frequency divided by 10.

Desired Baud Rate	Divisor Used to Generator 16 x Clock	Present Error Different Between Desired and Actual
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

Table 4. Baud Rates Using 3.072 MHz Crystal.

RS-232 Interface Specification

Signal Characteristics - EIA RS-232C

1. Receive

a. Mark	-3 to -25 volts
b. Space	+3 to +25 volts

2. Transmit

a. Mark	-8 volts with 3K ohm load
b. Space	+8 volts with 3K Ohm load

Maximum short circuit current	500 mA
Terminating Impendance	3K to 7K ohm

Signal Characteristics - Optional 20 mA Current Loop

When using the Teletype Model 33 or similar data terminal employing a current interface, the data terminal **MUST** be set up to operate in the Full-Duplex 20 Milliampere Neutral configuration. Refer to the related equipment manual for instructions.

TERMINAL Interface Pin Assignments - EIA RS-232C

Pin	Function
1	Protective Ground
2	Transmitted Data (Data In)
3	Received Data (Data Out)
5	Clear to Send
6	Data Set Ready
7	Signal Ground
8	Data Carrier Detector
20	Data Terminal Ready
16	Rdy/Busy Output (Rdy=0V, Busy=+5V)
25	Start/Stop Input (Start=0V, Stop=+5V)

(16 and 25 are optional features)

MODEM/CPU Interface Pin Assignments - EIA RS-232C

Pin	Function
1	Protective Ground
2	Transmitted Data (Data Out)
3	Received Data (Data In)
4	Request to Send
5	Clear to Send
7	Signal Ground
20	Data Terminal Ready
16	Rdy/Busy Output (Rdy=OV, Busy=+5V)
25	Start/Stop Input (Start=OV, Stop=+5V)

(16 and 25 are optional features)

The Modem/CPU interface cable and connector conform to EIA RS-232C and European CCITT V.24 standards and is a 25-pin (DB-25P) connector. The mating connector, located connector, located on the dataset or acoustic coupler, should be a DB-25S or equal. Signals to pins 4 and 20 are supplied by the SVI-805.

SYSTEM BLOCK DIAGRAM DESCRIPTION

As shown in STM-002-I, the primary function of the CRTC is to generate refresh addresses (MA0-MA13), row selects (RA0-RA4), and video monitor timing (HSYNC, VSYNC) and Display Enable. Other functions include an internal cursor register which generates a Cursor output when its contents compare to the current Refresh Address. A light-pen strobe input signal allows capture of Refresh Address in an internal light pen register.

All timing in the CRTC is derived from the CLK input. In alphanumeric terminals, this signal is the character rate. Character rate is divided down from video rate by external High Speed Timing when the video frequency is greater than 3 MHz. Shift Register, Latch, and MUX Control signals are also provided by external High Speed Timing.

The processor communicates with the CRTC through a buffered 8-bit Data Bus by reading/writing into the 18-register file of the CRTC.

The Refresh Memory address is multiplexed between the Processor and CRTC. Data appears on a Secondary Bus which is buffered from the processor Primary Bus. A number of approaches are possible for solving contentions for the Refresh Memory.

1. Processor always gets priority.

2. Processor gets priority access anytime, but can be synchronized by an interrupt to perform accesses only during horizontal and vertical retrace times.

3. Synchronize processor by memory wait cycles.

4. Synchronize processor to character rate (See Figure 4-6). The 6800 MPU family lends itself to this configuration because it has constant cycle lengths. This method provides zero burden on the processor because there is never a contention for memory. All accesses are "transparent".

The secondary data bus concept in no way precludes using the Refresh RAM for other purposes. It looks like any other RAM to the Processor. For example, using Approach 4, a 64K byte RAM Refresh Memory could perform refresh and programme storage functions transparently.

CRTC DESCRIPTION
(Figure STM-001-I: CRTC Block Diagram)

The CRTC consists of programmable horizontal and vertical timing generators, programmable linear address register, programmable cursor logic, light pen capture register, and control circuitry for interface to a processor bus.

All CRTC timing is derived from CLK, usually the output of an external dot rate counter. Coincidence (CO) circuits continuously compare counter contents to the contents of the programmable register file, RO-R17. For horizontal timing generation, comparisons result in: (1) Horizontal sync pulse (HS) of a frequency, position, and duration determined by the registers.

The Horizontal counter produces H clock which drives the Scan Line Counter and, Vertical Control. The contents of the Raster Counter are continuously compared to the Max Scan Line Address Register. A coincidence resets the Raster Counter and clocks the Vertical Counter.

Comparisons of Vertical Counter contents and Vertical Registers result in: (1) Vertical sync pulse (VS) of a frequency and position determined by the register - the width is fixed at 16 raster lines in the vertical control section and is not programmable, (2) Vertical Display of a frequency and position determined by the registers.

The Vertical Control Logic has other functions.

(1) Generate row selects, RAO-RA4, from the Raster Count for the corresponding interlace or non-interlace modes.

(2) Extend the number of scan lines in the vertical total by the amount programmed in the Vertical Total Adjust Register.

The Linear Address Generator is driven by CLK and locates the relative positions of characters in memory with their positions on the screen. Fourteen lines, MAO-MA13, are available for addressing up to four pages of 4K characters, 8 pages of 2K characters, etc. Using the Start Address Register, hardware scrolling through 16K characters is possible. The Linear Address Generator repeats the same sequence of addresses for each scan line of a character row.

The cursor logic determines the cursor location, size, and blinking rate on the screen. All are programmable.

The light pen strobe going high causes the current contents of the Address Counter to be latched in the Light Pen Register. The contents of the Light Pen Register are subsequently read by the Processor.

Internal CRTC registers are programmed by the processor through the data bus, DO-D7, and the control signals - R/$\overline{W}$, $\overline{CS}$, RS and E.

REGISTER FILE DESCRIPTION (See Table 2)

Nineteen registers in the CRTC can be accessed by means of the data bus. Register addressing and lengths are shown in Table 2.

Address Register

The Address Register is a 5-bit write-only register used as an "indirect" or "pointer" register. Its contents are the address of one of the other 18 registers in the file. When RS and $\overline{CS}$ are low, the Address Register itself is addressed. When RS is high, the Register File is accessed.

Horizontal Timing Registers RO, R1, R2 and R3

Figure 4-7 shows the visible display area of a typical CRT monitor giving the point of reference for horizontal registers as the left most displayed character position. Horizontal registers are programmed in "character time" units with respect to the reference.

Horizontal Total Register (RO) - This 8 bit write-only register determines the horizontal frequency of HS. It is the total of displayed plus non-displayed character time units minus one.

Horizontal Displayed Register (R1) - This 8 bit write-only register determines the number of displayed characters per horizontal line.

Horizontal Sync Position Register (R2) - This 8 bit write-only register determines the horizontal sync position on the horizontal line.

Horizontal Sync Width Register (R3) - This 4 bit write-only register determines the width of the HS pulse. It may not be apparent why this width needs to be programmed. However, consider that all timing widths must be programmed as multiples of the character clock period which varies. If HS width were fixed as an intergal number of character times, it would vary with character rate and be out of tolerance for certain monitors. The rate programmable feature allows compensating HS width.

VERTICAL TIMING REGISTERS R4, R5, R6, R7, R8 and R9

The point of reference for vertical registers is the top character position displayed. Vertical registers are programmed in character row times or scan line times.

Vertical Total Register (R4) and Vertical Total Adjust Register (R5) – The vertical frequency of VS is determined by both R4 and R5. The calculated number of character line times is usually an integer plus a fraction to get exactly a 50 or 60 Hz vertical refresh rate. The integer number of character line times minus one is programmed in the 7 bit write-only Vertical Total Register; the fraction is programmed in the 5 bit write-only Vertical Scan Adjust Register as a number of scan line times.

Vertical Displayed Register (R6) – This 7 bit write-only register determines the number of displayed character rows on the CRT screen, and is programmed in character row times.

Vertical Sync Position (R7) – This 7 bit write-only register determines the vertical sync position with respect to the reference. It is programmed in character row times.

Interlace Mode Register (R8) – This 2 bit write-only register controls the raster scan mode (see Figure 4-9). When bit and bit 1 are reset, or bit 0 is reset and bit 1 set, the non-interlace raster scan mode is selected. Two interlace modes are available. Both are interlaced sync raster scan mode is selected. Also when bit 0 and bit 1 are set, the interlace sync and video raster scan mode is selected.

Maximum Scan Line Address Register (R9) – This 5 bit write-only register determines the number of scan lines per character row including spacing. The programmed value is a max address and is one less than the number of scan lines.

OTHER REGISTERS

Cursor Start Register (R10) - This 7 bit write-only register controls the cursor format (see Figure 4-8). Bit 5 is the blink timing control. When bit 5 is low, the blink frequency is 1/16 of the vertical field rate, and when bit 5 is high, the blink frequency is 1/32 of the vertical field rate. Bit 6 is used to enable a blink. The cursor start scan line is set by the lower 5 bits.

Cursor End Register (R11) - This 5 bit write-only register sets the cursor end scan line.

Start Address Register (H & L) (R12, R13) - Start Address Register is a 14 bit write-only register which determines the first address put out as a refresh address after vertical blanking. It consists of an 8 bit lower register, and a 6 bit higher register.

Light Pen Register (H & L) (R16, R17) - This 14 bit read-only register is used to store the contents of the Address Register (H & L) when the LPSTB input pulses high. This register consists of an 8 bit lower and 6 bit higher register.

Cursor Register (H & L) (R14, R15) - This 14 bit read/write register stores the cursor location. This register consists of an 8 bit lower and 6 bit higher register.

CURSOR

The Cursor Start and End Registers allow a cursor of up to 32 scan lines in height to be placed on any scan lines of the character block as shown in Figure 10. Using Bits 5 and 6 of the Cursor Start Register, the cursor is programmed with blink periods of 16 or 32 times the field period. Optional non-blink and non-display modes can also be selected. When an external 2X blink on characters is required, it may be necessary to perform cursor blink externally as well so that both blink rates are synchronized. Note that an invert/non-invert cursor is easily implemented by programming the CRTC for blinking cursor and externally inverting the video signal with an exclusive-OR.

The cursor is positioned by changing the contents of registers R14 and R15. The cursor can be placed at any of 16K character positions, thus facilitating hardware paging and scrolling through memory without loss of the cursor's original position.

INTERLACE/NON-INTERLACE DISPLAY MODES

An illustration of the 3 raster scan modes of operation is hown in Figure 4-12 Normal sync mode is non-interlace. In this mode, each scan line is refreshed at the vertical field rate (e.g., 50 or 60 Hz). Frame time is divided into even and odd alternating fields. The horizontal and vertical timing relationship results in the displacement of scan lines in the odd field with respect to the even field. When the same information is painted in both fields, the mode is called "Interlace Sync," this is a useful mode for enhancing readability by filling in a character. When the even lines of a character are displayed in the even field and the odd lines in the odd field, the mode is called "Interlace Sync and Video". This last mode effectively doubles the character density on a monitor of a given bandwidth. The disadvantage of both interlace modes is an apparent flicker effect, which can be reduced by careful monitor design.

There are restrictions on the porgramming of CRTC registers for interlace operation:

(1) Horizontal total character count, N_{ht} must be odd (i.e., an even number of character times)

(2) For Interlace Sync and Video mode only, the max scan line address, N_{sl} , must be odd (i.e., an even number of scan lines)

(3) For Interlace Sync and Video mode only, the Vertical Displayed Total characters must be even. The programmed number, N_{vd}, must be one-half the actual number required.

(4) For Interlace Sync & Video mode only, the Cursor START and Cursor End Registers must both be even or both odd.

LIGHT PEN

The contents of the CRTC Address Counter are strobed into R16/R17 Light Pen Registers on the next high to low CLK transition after LPSTB goes high. In most systems, the light pen signal would also cause a processor interrupt routine to read R16/R17. Slow light pen response requires the processor software to modify the captured address read from R16/R17 by a calibration factor.

PROGRAMMING CONSIDERATIONS

Initialization – Registers RO-R15 must be initialized after power is turned on. The processor normally loads the CRTC registers sequentially from a firmware table. Henceforth, RO-R11 are not changed in most systems. The 6800 programme in Table 3 and Figure 12 shows a typical CRTC initialization.

Hardware Scrolling – Registers R12/R13 contents determine which memory location is the first displayed character on the screen. Since the CRTC Linear Address Generator counts from this beginning count, the displayed portion of the screen may be a window on any continuous string of characters within a 16K block or refresh memory. By centering the R12/R13 pointer in the middle of the available memory space, scrolling up or down is possible ... by line, page, or character.

6845 CRTC PIN DESCRIPTION

Processor Interface

The CRTC interfaces to a processor bus on the bidirectional data bus (DO-D7) using $\overline{CS}$, RS, E, and R/$\overline{W}$ for control signals.

Data Bus (DO-D7) – The bidirectional data lines (DO-D7) allow data transfers between the CRTC internal Register File and the processor. Data bus output drivers are 3-state buffers which remain in the high impedance state except when the processor performs a CRTC read operation. A high level on a data pin is a logical "1".

Enable (E) – The enable signal is a high impedance TTL/MOS compatible input which enables the data bus input/output buffers and clocks data to and from the CRTC. This signal is usually derived from the processor clock, and the high to low transition is the active edge.

Chip Select ($\overline{CS}$) – The $\overline{CS}$ line is a high impendance TTL/MOS compatible input which selects the CRTC when low to read or write the internal Register File. This signal should only be active when there is a valid stable address being decoded from the processor.

Register Select (RS) - The RS line is a high impendance TTL/MOS compatible input which selects either the Address Register (RS = "0") or one of the Data Registers (RS = "1") of the internal Register File.

Read/Write (R/$\overline{W}$) - The R/$\overline{W}$ line is a high impedance TTL/MOS compatible input which determines whether the internal Register File gets written or read. A write is active low ("0").

CRT CONTROL

The CRTC provides horizontal sync (HS), vertical sync (VS), and Displayed Enable signals.

Vertical sync (V SYNC) - This TTL compatible output is an active high signal which drives are monitor directly or is fed to Video Processing Logic for composite generation. This signal determines the vertical position of the displayed text.

Horizontal Sync (H SYNC) - This TTL compatible output is an active high signal which drives the monitor directly or is fed to Video Processing Logic for composite generation. This signal determines the horizontal position of the displayed text.

Display Enable - This TTL compatible output is an active high signal which indicates the CRTC is providing addressing in the active Display Area.

REFRESH MEMORY/CHARACTER GENERATOR ADDRESSING

The CRTC provides Memory Addresses (MA0-MA13) to scan the Refresh RAM. Also provided are Raster Addresses (RA0-RA4) for the character ROM.

Refresh Memory Addresses (MA0-MA13) - These 14 outputs are used to refresh the CRT screen with pages of data located within a 16K block of refresh memory. These outputs drive a TTL load and 30pF. A high level on MA0-MA13 is a logical "1".

Raster Addresses (RA0-RA4) - These 5 outputs from the internal Raster Counter address the Character ROM for the row of a character. These outputs drive a TTL load and 30pF. A high level (on RA0-RA4) is a logical "1".

OTHER PINS

Cursor – This TTL compatible output indicates Cursor Display to external Video Processing Logic. Active high signal.

Clock (CLK) – The CLK TTL/MOS compatible input is used to synchronize all CRT control signals. An external dot counter is used to derive this signal which is usually the character rate in an alphanumeric CRT. The active transition is high to low.

Light Pen Strobe (LPSTR) – This high impendance TTL/MOS compatible input latches the current Refresh Addresses in the Register File. Latching is on the low to high edge and is synchronized internally to character clock.

V_{CC}, G

$\overline{RES}$ – The $\overline{RES}$ input is used to Reset the CRTC. An input low level on $\overline{RES}$ forces CRTC into following status:

(A) All the counters in CRTC are cleared and the device stops the display operation.

(B) All the outputs go down to low level.

(C) Control registers in CRTC are not affected and remain unchanged.

This signal is different from other 6800 family in the following functions:

(A) $\overline{RES}$ signal has capability of reset function only when LPSTB is at low level.

(B) After $\overline{RES}$ has gone down to low level, output signals of MA0-MA13 and RA0-RA4, synchronizing with CLK low level, goes down to low level. (At least 1 cycle CLK signal is necessary for reset.)

(C) The CRTC starts the Display operation immediately after the release of $\overline{RES}$ signal.

$\overline{RES}$	LPSTB	OPERATING MODE
0	0	Reset
0	1	Test Mode
1	0	Normal Mode
1	1	Normal Mode

ILLUSTRATION OF THE CRT SCREEN FORMAT

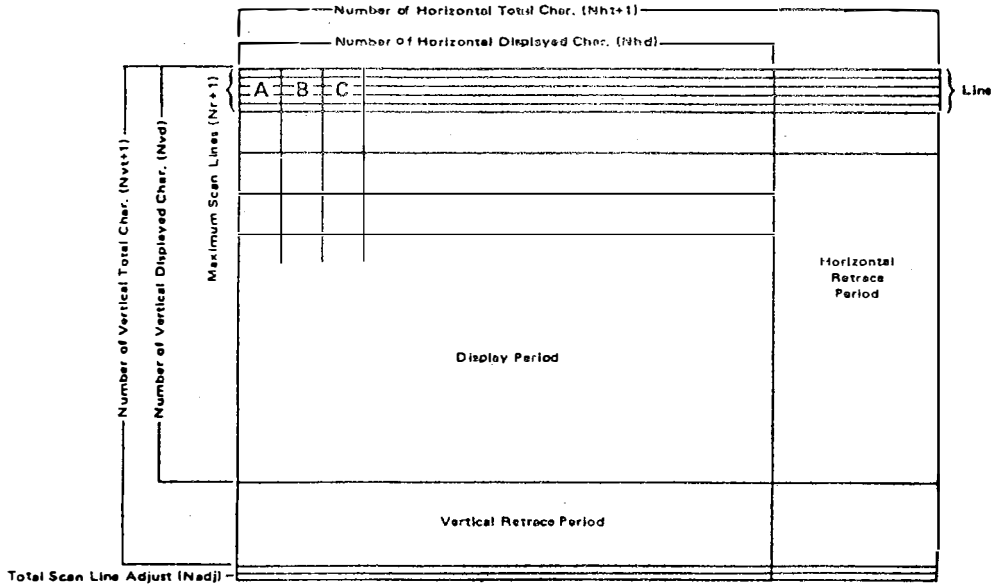
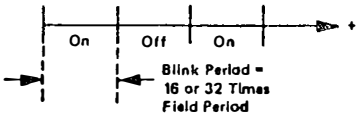


FIG. 4-7

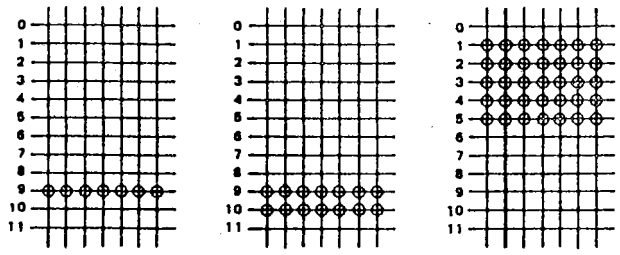
CURSOR CONTROL

Cursor Start Register

B Bit 6	P Bit 5	Cursor Display Mode
0	0	Non-Blink
0	1	Cursor Non-Display
1	0	Blink, 1/16 Field Rate
1	1	Blink, 1/32 Field Rate



Example of Cursor Display Mode



Cursor Start Adr. = 9
Cursor End Adr. = 0

Cursor Start Adr. = 9
Cursor End Adr. = 10

Cursor Start Adr. = 1
Cursor End Adr. = 5

FIG. 4-8

INTERFACE CONTROL

Interlace Mode Register

Bit 1	Bit 0	Mode
0 1	0 0	Normal Sync Mode (Non-Interlace)
0	1	Interlace Sync Mode
1	1	Interlace Sync & Video Mode

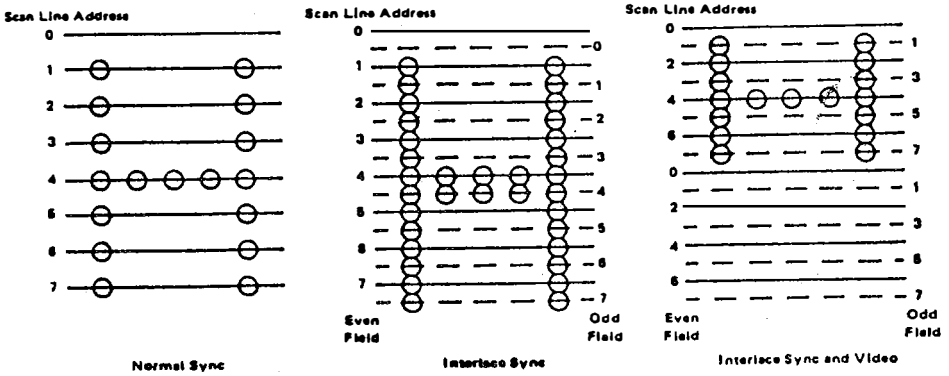


FIG. 4-9

TABLE 2 – CRTC INTERNAL REGISTER ASSIGNMENT

		Address Register					Register					Number of Bits							
$\overline{CS}$	RS	4	3	2	1	0	#	Register File	Programme Unit	Read	Write	7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	-	-	-	-								
0	0	X	X	X	X	X	X	Address Register	-	No	Yes								
0	1	0	0	0	0	0	R0	Horizontal Total	Char.	No	Yes								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Char.	No	Yes								
0	1	0	0	0	1	0	R2	H. SYnc Position	Char.	No	Yes								
0	1	0	0	0	1	1	R3	H. Sync Width	Char.	No	Yes								
0	1	0	0	1	0	0	R4	Vertical Total	Char. Row	No	Yes								
0	1	0	0	1	0	1	R5	V. Total Adjust	Scan Line	No	Yes								
0	1	0	0	1	1	0	R6	Vertical Displayed	Char. Row	No	Yes								
0	1	0	0	1	1	1	R7	V. Sync Position	Chr. Row	No	Yes								
0	1	0	1	0	0	0	R8	Interlace Mode	-	No	Yes								

0	1	0	1	0	0	1	R9	Max Scan Line Address	Scan Line	No	Yes	
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line	No	Yes	B P (Note 1)
0	1	0	1	0	1	1	R11	Cursor End	Scan Line	No	Yes	
0	1	0	1	1	0	0	R12	Start Address (H)	-	No	Yes	
0	1	0	1	1	0	1	R13	Start Address (L)	-	No	Yes	
0	1	0	1	1	1	0	R14	Cursor (H)	-	Yes	Yes	
0	1	0	1	1	1	1	R15	Cursor (L)	-	Yes	Yes	
0	1	1	0	0	0	0	R16	Light Pen (H)	-	Yes	No	
0	1	1	0	0	0	1	R17	Light Pen (L)	-	Yes	No	

Note 1 : Bit 5 of the Cursor Start Register is used for blink period control, and Bit 6 is used to select blink or non-blink.

FD1793 FLOPPY DISK CONTROLLER DESCRIPTION

The Floppy Disk Formatter block diagram (STM-003-C). The primary sections include the parallel processor interface and the Floppy Disk interface.

DATA SHIFT REGISTER - This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

DATA REGISTER - This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

TRACK REGISTER - This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

SECTOR REGISTER (SR) - This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

COMMAND REGISTER (CR) - This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

STATUS REGISTER (STR) - This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC LOGIC - This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). the polynomial is:

$$G(x) = x^{16} + x^{12} + x^5 + 1$$

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

ARITHMETIC/LOGIC UNIT (ALU) - The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

TIMING AND CONTROL - All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1791/3 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0, double density (MFD) is assumed. When $\overline{DDEN}$ = 1, single density (FM) is assumed. MFM

AM DETECTOR - The address mark detector detects ID, data and index address marks during read and write operations.

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD1793. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is ready by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force interrupt command condition is met.

FLOPPY DISK INTERFACE

The 1793 has two modes of operation according to the state of $\overline{\text{DDEN}}$ (Pin 37). When $\overline{\text{DDEN}}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM ro MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1". For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0". Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track as far as the FD179 is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179 is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table)

For read operations, the FD1793 requires $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD1793 must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD1793 is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD1793 must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{\text{VFOE}}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{\text{VFOE}}$ will go active when:

(a) Both HLT and HLD are True
(b) Setting Time, if programmed, has expired
(c) the 1793 is inspecting data off the disk

If $\overline{\text{WF}}/\overline{\text{VFOE}}$ is not used, leave open or tie to a 10K resistor to +5.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/White head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD1793 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1793 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD1793 provides Write Gate (Pin 30) and Write Date (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{\text{DDEN}}$ = 1) and 250 ns pulses in MFM ($\overline{\text{DDEN}}$ = 0). Write Data provides the unique address marks in both formats.

Also duridng write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD1793. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

WRITE PRECOMPENSATION

Write precompensation (which counteracts the 'drifting' when flux transitions are placed close together on the more cramped inside tracks) is available to the user on any tracks that he feels necessary.

STATUS REGISTER SUMMARY

BIT	ALL TYPE 1 COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE 1 COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TR00}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
SO BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

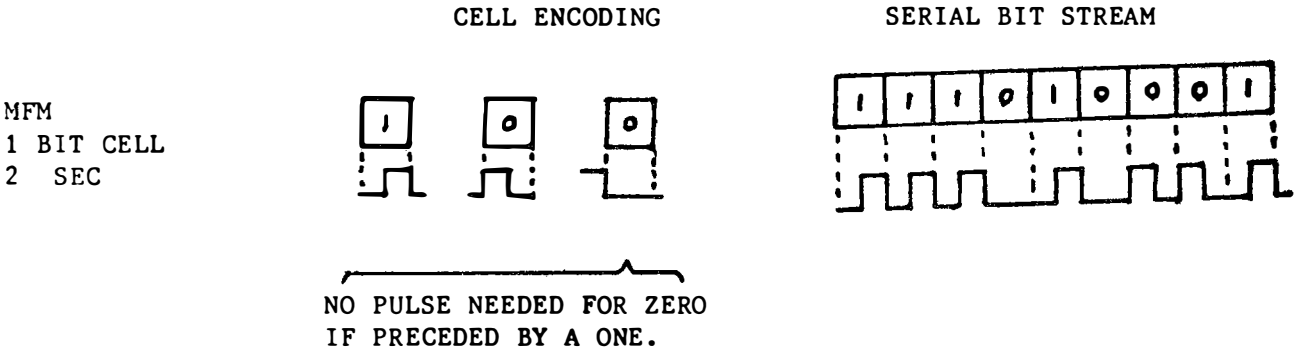
BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
SO BUSY	When set, command is under execution. When reset, no command is under execution.

Data Organization on the Disc Media

The disc cartridge contains a magnetic oxide-coated disc, which is visible through access holes in the plastic jacket. The host system, through the Disc Drive, records data on the disc at addressed locations. Given the address of data on the disc, the read/write head quickly locates and retrieves the desired data. As the disc spins, serial binary data is recorded (or read) on concentric circles called tracks. Below picture shows track 00 on the outer edge of the disc; the innermost track is track 40. Each of the tracks is divided into sectors, which are marked by one hole punched in the disc. An additional hole, INDEX, occurs approximately 180 degrees before sector 0 (sector location depends upon the relative position of the read/write head and the index sensor). Each track starts with a pulse initiated by the Index hole while each sector starts by a pulse initiated by a sector hole. Notice that the physical length of sectors varies directly in proportion to the distance of the track from the center of the disc, data bits are closer together on the higher numbered tracks.

Double Density

Double capacity can be obtained by use of MFM (modified frequency modulation) method of encoding data on the disc.



MFM disc encoding format.

FUNCTIONAL OPERATIONS

The following paragraphs define the functional as well as the timing relationships of the operations for the SA200.

Power Sequencing

Applying dc power to the SA200 can be done in any sequence. However, during power-up, the WRITE GATE line must be held in active or at a high level. This will prevent possible "glitching" of the media. After application of dc power, a 350 ms delay should be introduced before any operation is performed. After powering on, initial position of the read/write head with respect to the data tracks on the media can be read in the header ID field. In order to assure proper positioning of the read/write head after powering on, a step out operation should be performed until the TRACK 00 line becomes active (recalibrate).

Drive Selection

Drive selection occurs when the appropriate DRIVE SELECT line is activated and the proper select jumper block is installed.

Motor On

In order for the host system to read or write data, the dc drive motor must be turned on. This is accomplished by activating the MOTOR ON line. A 350 ms delay must be introduced after activating this line to allow the motor to come up to speed before reading or writing can be accomplished.

The motor must be turned off by the host system by deactivating the MOTOR ON line. This should be done if the drive ha not received a new command within 2 seconds (10 revolutions of diskette) after completing the execution of the last command. This ensures maximum motor and media life.

Track Accessing

Seeking the read/write head from one track to another is accomplished by:

(a) WRITE GATE being inactive.

(b) Activating the DRIVE SELECT line.

(c) Selecting the desired direction using the DIRECTION SELECT line.

(d) Pulsing the STEP line.

Multiple track accessing is accomplished by repeatedly pulsing the STEP line until the desired track has been reached. Each pulse on the STEP line will cause the read/write head to move either one track in or one track out, depending on the DIRECTION SELECT line. DIRECTION SELECT is triggered by the trailing edge of the step pulse. Head movement is initiated on the trailing edge of the step pulse.

Step Out

With the DIRECTION SELECT line at a logical one level (2.5 to 5.25V), a pulse on the STEP line will cause the read/write head to move either one track away from the centre of the disk towards track 00.

Step In

With the DIRECTION SELECT line at a minus logic level (0 to 0.4V), a pulse on the STEP line will cause the read/write head to move one track closer to the centre of the disk towards track 39.

PIN NO.	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	$\overline{\text{MASTER RESET}}$	$\overline{MR}$	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V +-5%
40		V_{DD}	+12V +-5%
COMPUTER INTERFACE:			
2	$\overline{\text{WRITE ENABLE}}$	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	$\overline{\text{CHIP SELECT}}$	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	$\overline{\text{READ ENABLE}}$	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5,	REGISTER SELECT	A0, A1	These inputs select the register to receive transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control:

A1	A0	$\overline{RE}$	$\overline{WE}$
0	0	Status Reg	Command Reg
0	1	Track Reg	Track Reg
1	0	Sector Reg	Sector Reg
1	1	Data Reg	Data Reg

PIN NO.	PIN NAME	SYMBOL	FUNCTION
7-14	$\overline{\text{DATA ACCESS LINES}}$	$\overline{\text{DAL0}}$-$\overline{\text{DAL7}}$	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{\text{WE}}$ or transmitter enabled by $\overline{\text{RE}}$.
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for mini-drives.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occuring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occuring while Late is active (high) should be shifted late for write precompensation.

PIN NO.	PIN NAME	SYMBOL	FUNCTION
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged.
25	READ GATE (1791/3)	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchroniczation.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S = 1, SSO is set to a logic 1. When S = 0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.

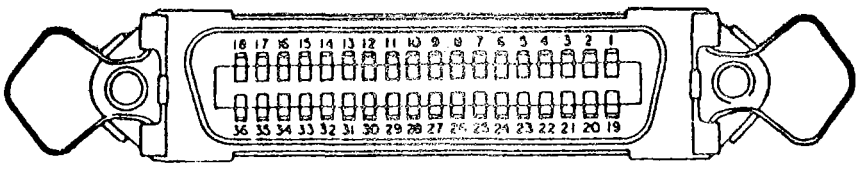
PIN NO.	PIN NAME	SYMBOL	FUNCTIONS
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per its transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readliness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bid 7.
33	$\overline{\text{WRITE FAULT}}$ $\overline{\text{VFO ENABLE}}$	$\overline{\text{WF}}/\overline{\text{VFOE}}$	This is a bidirectional signal used to signify writing faults at the drive, and to enable the external PLD data separator. When WG = 1, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD179X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the FD179X when the index hole is encountered on the diskette.

PIN NO.	PIN NAME	SYMBOL	FUNCTION
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected. This line must be left open on the 1792/4.

CENTRONICS INTERFACE

1. Input/Output Connector

Use a conncetor, AMP CHAMP 36 BAIL LOCK TYPE, to input data into the Printer. Pin configuration and its signals of the receptacle in left rear of the Printer are described below.



PIN	SIGNAL	PIN	SIGNAL
1	$\overline{\text{STRPNE}}$	19	TWISTED PAIR GND (PAIR WITH 1 PIN)
2	DATA 1	20	TWISTED PAIR GND (PAIR WITH 2 PIN)
3	DATA 2	21	TWISTED PAIR GND (PAIR WITH 3 PIN)
4	DATA 3	22	TWISTED PAIR GND (PAIR WITH 4 PIN)
5	DATA 4	23	TWISTED PAIR GND (PAIR WITH 5 PIN)
6	DATA 5	24	TWISTED PAIR GND (PAIR WITH 6 PIN)
7	DATA 6	25	TWISTED PAIR GND (PAIR WITH 7 PIN)
8	DATA 7	26	TWISTED PAIR GND (PAIR WITH 8 PIN)
9	DATA 8	27	TWISTED PAIR GND (PAIR WITH 9 PIN)
10	$\overline{\text{ACK}}$	28	TWISTED PAIR GND (PAIR WITH 10 PIN)
11	BUSY	29	TWISTED PAIR GND (PAIR WITH 11 PIN)
12	GND	30	GND
13	NC	31	$\overline{\text{INITIAL}}$ (PAIR WITH 14 PIN)
14	GND	32	$\overline{\text{ERROR}}$ (PAIR WITH 15 PIN)
15	GND	33	GND
16	GND	34	$\overline{\text{CLK}}$ (PAIR WITH 33 PIN)
17	CHASSIS GND	35	$\overline{\text{TEST}}$ (PAIR WITH 16 PIN)
18	+5V 80mA Maximum	36	+5V

Note: 1. The combined output of pins 18 and 36 is 80mA maximum.
2. NC stands for no connection.

2. Input/Output Signals

(1) Input signals to the Printer

* DATA 1
  DATA 2
  DATA 3
  DATA 4
  DATA 5
  DATA 6
  DATA 7
  DATA 8

  8-bit data signals.
  Signal "HIGH" represents Logic '1'.

* $\overline{\text{STROBE}}$ — This strobe signal is used to read in 8 bits of data. Data is read in when the signal goes 'LOW'.

* $\overline{\text{INITIAL}}$ — This signal is used to set the Printer to an initial state and is normally "HIGH". Bringing the line "LOW" and returning it "HIGH" starts the clearing action which sets the Printer to an initial state.

* $\overline{\text{TEST}}$ — This signal is used for the self-printing test which is executed by bringing the line "LOW".

(2) Output signals from the Printer

* BUSY — This signal indicates the BUSY status of the Printer. When "HIGH" the Printer cannot accept data.

* $\overline{\text{ACK}}$ — This signal is used to indicate that the Printer is awaiting data.

Note: The BUSY and $\overline{\text{ACK}}$ signals are always output when the Printer accepts data input.

* $\overline{\text{ERROR}}$ — A printer error condition causes this signal to go "LOW". When this happens all the control circuits internal to the Printer halt. Ther are two ways to correct this situation.

  - Turn the Printer off - and then back on two seconds later.

  - Input the $\overline{\text{INITIAL}}$ signal

  An ERROR occurs if the dot timing goes bad.

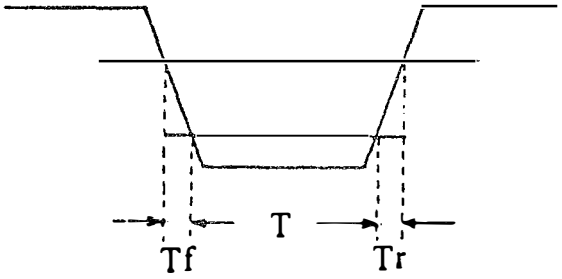
* $\overline{\text{CLK}}$ — This is a 400 KHz clock signal. It can be used with an interface if needed.

(3) Electrical Characteristics

(1) Signal levels

All input/output signals are TTL level.

"HIGH" level ..... +2.4 - 5.0V
"LOW" level ..... +0.0 - 0.4V at the Printer input terminals



Tf and Tr = 100 ns or less
T ≒ value shown on the timing chart

(2) Input/Output conditions

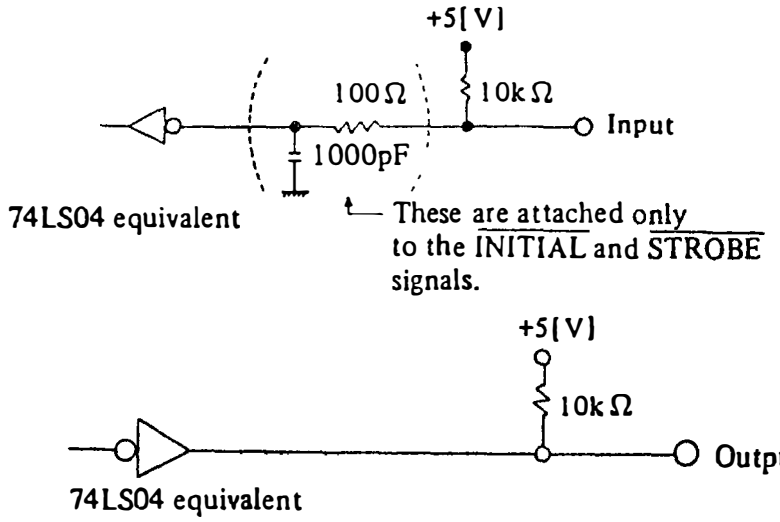
Input/output signals are pulled up with 10 k ohms.

* Input signals

The input load corresponds to one 74LS04

* Output signals

The output corresponds to a 74LS04. The recommended output load corresponds to one LSTTL load.



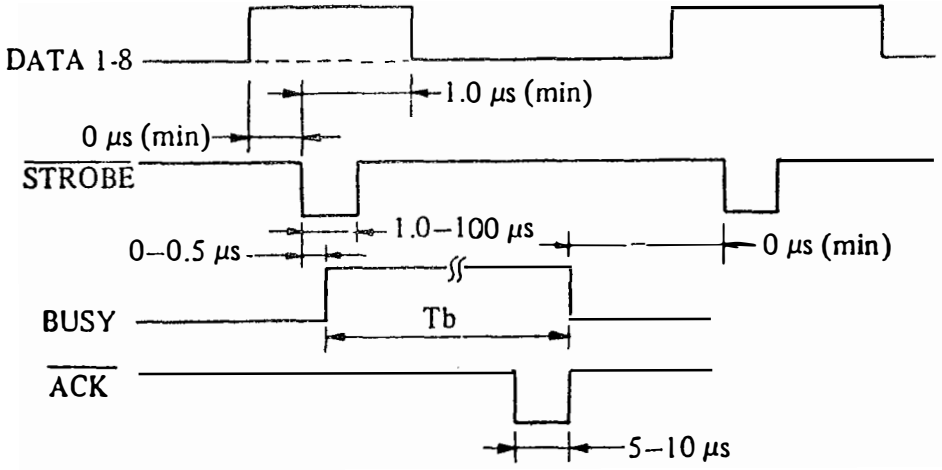
(3) Signal cable length

Maximum length is two meters with the following signals forming twisted pairs with the GND.

$\overline{\text{STROBE}}$, $\overline{\text{INITIAL}}$, BUSY, $\overline{\text{ACK}}$, $\overline{\text{ERROR}}$, $\overline{\text{CLK}}$

(4) Timing Chart

(1) Data input

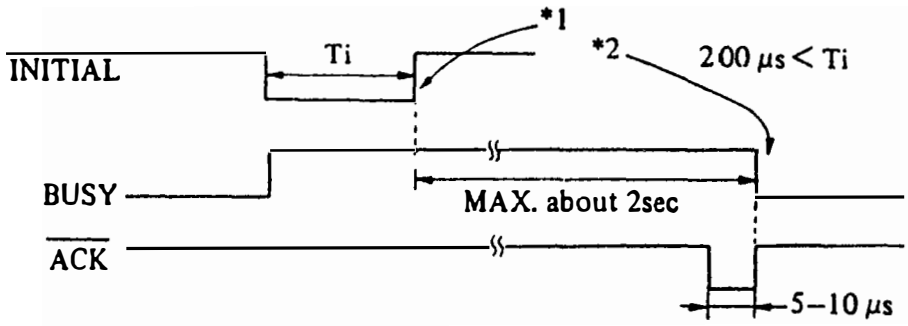


Tb; CHARACTER CODE
CR/NL/DC4 CODE

100 s or more
PRINTER + CARRIAGE RETURN
(about 3 seconds maximum)

Reference: CR = (o, D), NL = (O, A), DC4 = (1, 4)

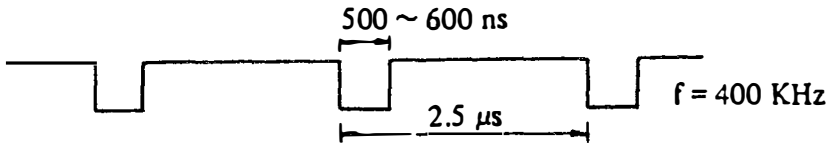
(2) $\overline{\text{INITIAL}}$ signal input timing



*1 During Ti, the $\overline{\text{INITIAL}}$ line is "LOW" and the printer is held in a reset state. The initialization sequence starts execution after the line goes "HIGH".

*2 After the Printer finishes execution of the initialization sequence the BUSY line goes "LOW".

(3) $\overline{\text{CLK}}$ signal



(5) Self-Test Printing

Bringing the $\overline{\text{TEST}}$ line "LOW" starts the self-test printing which continues until it is returned "HIGH".

(6) Chasis Ground

As stated in [6]-3-(3), all of the signal lines should be twisted pairs with the signal ground lines, but it is further recommended that the cable be shielded and that one terminal be connected to the CONTROLLER CHASSIS GND and the other connected to the FRAME GND on the controller side.

5. CIRCUIT SCHEMATIC AND COMPONENT LAYOUT